Indian Journal of Engineering & Materials Sciences
Vol. 27, August 2020, pp. 916-920

Simulation of the process variation in negative capacitance virtual-source carbon nanotube FET devices and circuits

Bharathi Raj Muthu[a*], Ewins Pon Pushpa Solomon[a] & Vaithiyanathan Dhandapani[b]

[a]Department of Electronics and Communication Engineering, College of Engineering Guindy, Anna University, Chennai 600 025, Tamil Nadu, India

[b] Department of Electronics and Communication Engineering, National Institute of Technology Delhi, Delhi 110 040, India

Received: 26 May 2020

We have reported the impact of process variation of virtual- source carbon nanotube field-effect transistor (VS-CNFET) device externally connected to the epitaxial ferroelectric (FE) capacitor through the spectre parametric simulation. We have found that the FE materials with high remnant polarization produces better transfer characteristics and suppressed short channel effects (SCE). The increase in the ferroelectric thickness (t_{fe}) has brought out the good impact of 4x improvement in ON current and reduced subthreshold swing of 40 mV/decade. The ON current has been increased with increase in thickness of ferroelectric material and has followed a monotonic trend, where the leakage current becomes a major concern and optimization of crucial parameters such as a diameter of the nanotube has given importance. Relative to the VS- CNFET model, the negative capacitance VS-CNFET model has stacked in ring oscillator (RO) displays immune to delay variation and produces better switching characteristics.

Keywords: Carbon nanotube field effect transistors, Ferroelectric, Negative capacitance, Short channel effects

1 Introduction

One of the critical aspects of semiconductor processing is continuing Moore's scaling trends which are limited by the process variation challenges[1]. Thus, building the high- performance architecture without many processes and temperature variation becomes a complex task[2]. Random doping fluctuations, variation related to the gate dielectric, strain, implant, annealing, and patterning effects are the major critical variation factors[3]. Recently, Negative capacitance (NC) effect exhibited by the Ferroelectric (FE) materials brings hope to further miniaturization and become the solution for the sub-20 nm technological constraints[4]. The spontaneous polarization effect displayed by the FE materials develops a passive amplification, thus the sub-threshold swing (SS) lowered to sub 60mV/decade of Boltzmann definition[5]. The NC effect is explored with unique features in the recently developed experimental negative capacitance FETs (NCFET) and analyzed with the variation in work function engineering and for varying FE materials[6-8]. FinFET has become a one of the most promising multigate transistor device which helps to eradicate the short channel effects[9]. The FinFET device is externally connected to an FE capacitor and reports SS of about 8.5 mV/decade with eight orders of increase in the magnitude of drain current (I_D). Also, hysteresis is taken as a major concern and measures are taken to reduce it to as low as 0.48 V[10-12]. With interest in emerging 2D materials, the NC concept is applied to the carbon nanotube FETs which shows SS of 55 mV/decade and 2.1x times increase in drain current[13].

Attaining the stable polarization for thin ferroelectrics is a major concern and destabilizing the polarization causes negative electrical permittivity when stacked in the heterostructure[14]. The recent 30 nm contact gate pitch suitable for sub-3 nm technology node provides 1.6x times increase in Energy delay product (EDP) compared to conventional CNFET[15]. The above-mentioned study focuses on the impact of FE thickness on the novel current-voltage characteristics and the impact of varying FE material externally driving the CNFET model provides various insights into the aforementioned characteristics and its second order effects (SOE). In this work, we use cadence spectre circuit simulator to investigate the transfer characteristics, SCE, temperature effects for a process variation of CNFET, and the thickness of the FE

*Corresponding author (E-mail: mbharathiraj@annauniv.edu.in)

material. Section II describes the modeling approach of NC-CNFET model, the impact of varying FE capacitor is discussed in Section III, and in Section IV thickness of NC-CNFET model. In Section V and VI, the process variation in CNFET with respect to t_{fe} with its circuit performance is provided.

2 NC-CNFET modeling approach

The semi-empirical VS-CNFET model is used to determine charge-voltage and current-voltage characteristics in sub-20 nm short channel MOSFET. It is coupled with the Landau-Khalatnikov (L-K) equation derived for the ferroelectric material based capacitor. The baseline VS-CNFET model uses the 14 nm technology node and the model card, describing the 14 nm CNFET technology node in VERILOG-A file contains the following geometrical and process parameters are Gate Length L_g = 18 nm, Contact length L_c = 18 nm, Source/Drain extension length L_{ext} = 3 nm, Gate height H_g = 20 nm, Oxide thickness t_{ox} = 0.9 nm, diameter of nanotube d = 1.2 nm, spacing between nanotubes s= 10 nm are extracted from the experimental calibrated data and International technology roadmap for semiconductors (ITRS) suggestions[16-19]. The FE materials with high remnant polarization like Barium titanate ($BaTiO_3$), Hafnium (IV) silicate (HfSiO), Strontium Bismuth Tantalate (SBT), Lead zirconate titanate (PZT), and Polyvinylidene fluoride (PVDF) are used with t_{fe} ranging from 600 to 1000 nm[10, 20]. Figure 1 shows the symbolic representation of baseline CNFET which is externally connected to the negative capacitor.

3 Impact of varying ferroelectric capacitors driving VS-CNFET

The non-linear electric property of FE oxide exhibit spontaneous polarization below its Curie temperature (T_C) and can be altered by an externally applied electric field. Reversibility of the polarization is the key feature of the FE material which develops a hysteresis loop (P-E). Also, it displays two stable polarization states which can be used for memory device applications such as FE random access memory. Some of the barium strontium titanate (BST) ceramics tends to change its dielectric constant near the T_C with an externally applied electric field. Thus, it is possible to use it for electrically tunable devices and a non-volatile memory device which is compatible with CMOS and carbon nanotube (CNT) technology[21]. Sandwiching of FE material between the gate and dielectric stack creates passive amplification of the electric field and in turn, reduce the overall supply voltage[4].

The FE materials with high remnant polarization are chosen to model the capacitors driving the CNFET externally to determine the transfer characteristics and SCE[13,22]. The t_{fe} is fixed to 1 μm with the operating voltage of about 0.4 V[17]. The PVDF and $HFSiO_4$ show excellent variation providing early threshold voltage with high ON current compared to the reference CNFET model extracted from the input characteristics plotted between the drain current (I_{DS}) vs. Gate to source voltage (V_{GS}) Fig. 2(a & b). Also, there is a 4x time's increase in the saturation current for the PVDF based

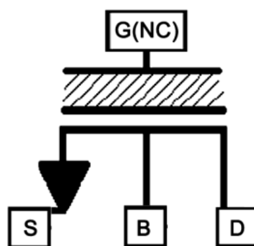

Fig. 1 — Symbolic representation of the nmos Negative capacitance carbon nanotube field effect transistor where the Ferroelectric dielectric is connected externally.

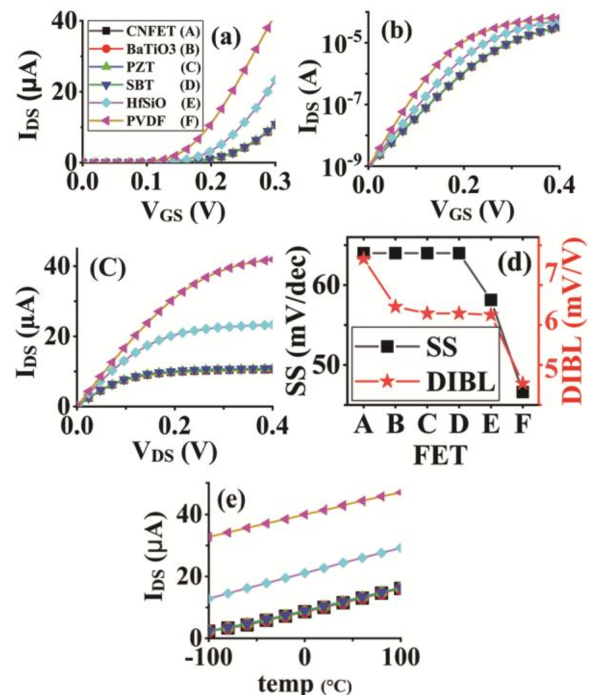

Fig. 2 — (a) I_{DS}–V_{GS} characteristics of n-type NC-CNFETs driven by externally connected capacitor made of different ferroelectric materials at V_{DD} = 0.4 V, (b) ON current variation, (c) I_{DS}–V_{DS}plots of NC-CNFETs with t_{fe}= 1 μm (/V_{GS}/ is varied from 0 to V_{DD}), (d) The measure of SS & DIBL and (e) Temperature effects.

CNFET model extracted from the output characteristics for the drain current (I_{DS}) versus Drain-to-source voltage (V_{DS}) Fig. 2(c). The decrease in the SS from 63 mV/decade to 47 mV/decade, Drain induced barrier lowering (DIBL) from 7 mV/V to 4.75 mV/V and the temperature effects showing drain current for maximum V_{GS} & V_{DS} at 1 µm of t_{fe} is shown in Fig. 2(d & e).

4 Impact of thickness of Fe material in H_FSIO & PVDF based CNFET

As the film thickness increases it develops strong dipole moments with an increase in spontaneous polarization. An enlarged t_{fe} brings out huge advantages in drain current, scaling of bias voltage, and improved SCE[23]. Recently, the experimental NC-FinFET showed good improvement in the increase of drain current from 7 to 9 orders of magnitude for the range of 100–300 mV of gate voltage, hysteresis window of near 5 V, and extremely low SS of 8.5–40 mV/decade[24]. For the t_{fe} less than 300 nm, the transient current becomes broader and slows down the switching. The aluminium oxide (Al_2O_3) stacked between the aluminum electrode and the FE film acts as a surface oxidation layer causing depolarization field and affects the switching. Hence, it is evident that the thinner the FE film, more the depolarization field. It is necessary to set the t_{fe} to produce a near coercive field of the corresponding FE material to trigger the fast switching[25]. The high-K $HfSiO_2$ gate dielectric provides improved I_{ON}/I_{OFF} ratio of 10^8, SS of 65 mV/decade and DIBL of 15 mV/V[26]. For further improvisation, the technique of externally connected capacitor which provides 59 mV/decade of SS and 6 mV/V of reduced DIBL[10]. Fig. 3(a & e) shows the comparative results of I/O characteristics, SS-DIBL, I_{ON}-I_{OFF}, and temperature effects of PVDF and $HfSiO_4$ based capacitor driving VS-CNFET. The obtained results were compared with the experimental values of integrated negative capacitance CNFET and the externally connected capacitor overrules the integrated model[13].

5 Process variation in CNFET for varying ferroelectric thickness

The geometric parameter created a huge impact in the process variations and hence the parametric analysis was made one parameter at a time for varying t_{fe}. The width (W), the spacing between tubes (s), the diameter of the nanotube (d), the gate length (L_g), and oxide thickness (t_{ox}) provides excellent electrostatic charge control in sub-10 nm technology node. The diameter of the nanotube is related to the band gap i.e $E_g = 2E_P a_{cc}/d$, where E_P = 3 eV, a_{cc} = carbon-carbon distance. Furthermore, the quantum capacitance increases with a decrease in diameter, except for the mobility which follows a monotonic trend[18]. The 1 nm thin sheet of carbon forms the nanotube where the negative capacitance effect further boosts the electrostatic charge control and high carrier mobility as shown in Fig. 4(a & c). To drive high capacitance loads, it is necessary to generate sufficient driving current. In the CNFET model, the capacitance of the CNFET is proportional to the number of nanotubes (N).

As the spacing between the tubes was reduced with s < 2d, there was a significant loss in capacitance and in turn, reduces the current per tube. If this loss is greater than the load capacitance, then there is an increase in delay. Thus, an optimal spacing of 10 nm is chosen with respect to the parasitic capacitance is fixed to reduce delay[27]. The improved ON current, SCE and temperature effects are shown in Fig. 4(d & f). The Schottky barrier (SB) CNFET model developed to suppress the ambipolar conduction is

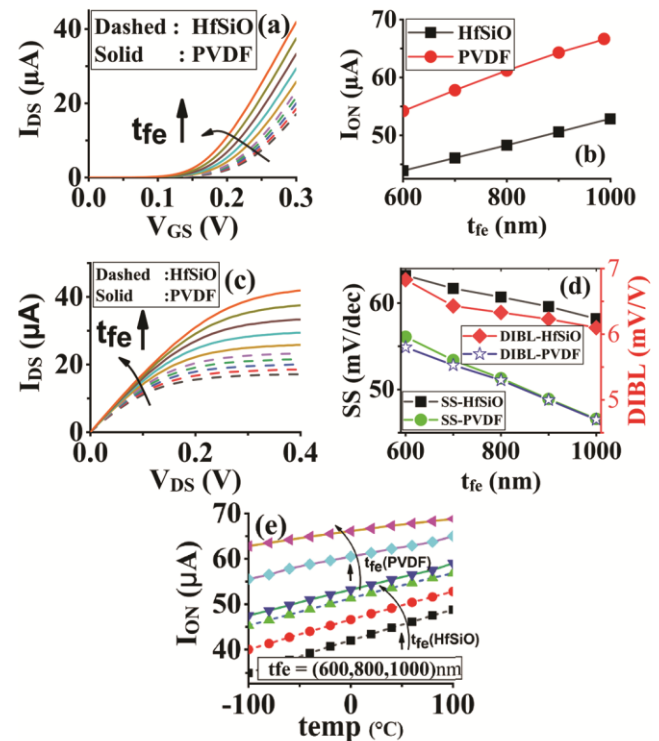

Fig. 3 — (a) Comparative analysis of I_{DS}–V_{GS} characteristics of PVDF and HfSiO FE stacked capacitor driving NC-CNFET at V_{DD} = 0.4V, (b) ON current variation, (c) I_{DS}–V_{DS} plots of NC-CNFETs (/V_{GS}/ is varied from 0 to V_{DD}), (d) The measure of SS and DIBL and (e) Temperature effects.

still likely to have leakage current with respect to supply voltage and for the larger diameter. As the t_{ox} is thicker, it can be suppressed by reducing the SB height to zero. But for thinner t_{ox}, the CNFET is still ambipolar irrespective of the SB height. Heavily doped source/drain CNFET could suppress this effect with a reduction in leakage current ranging from µA to nA. Better electrostatic charge control, reduced leakage and hysteresis loop are the key benefits of reducing the t_{ox} in CNFET[28]. The NC does not affect the leakage current rather it increases the ON current for reduced t_{ox} Fig. 4(g & i). The width of the transistor depends on the pitch and number of nanotubes used in the device and is given by W_{gate}= max (W_{min} , N * pitch). Both spacing and width were correlated with one another as the numbers of nanotubes tend to increase with reduced spacing and the overall gate width determines the transistor width[29] as shown in Fig. 4(j & l). The scaling of transistor length is limited due to intrinsic CNT's and the further scaling is boosted by doping source/drain CNTs. In the experimental CNFET, the channel length in the range from 3 µm to 15 nm is chosen[30]. For the range of 10–100 nm, L_g shows good variation in the ON current which is shown in Fig. 4(m & o). Finally, the externally connected negative capacitance CNFET is applied in the 7-stage ring oscillator circuit which produces reduced delay at an operating voltage of 75mV is shown in the Fig. 5.

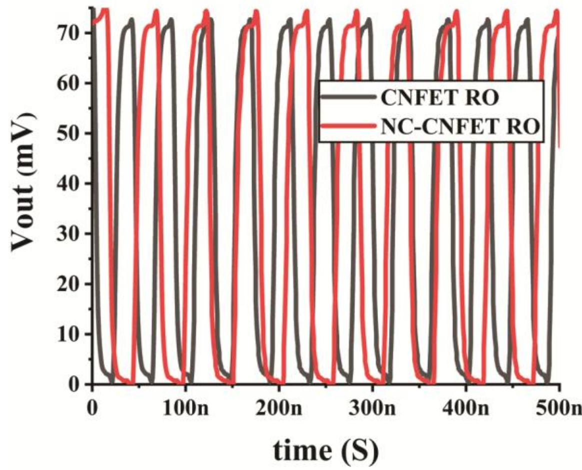

Fig. 5 — 7-stage ring-Oscillator showing variation in delay between VS-CNFET model and negative capacitance VS- CNFET model.

6 Conclusions

We have reported the effects of the transient characteristics, SCE and the process variability with respect to the t_{fe} for the virtual source CNFET model driven by the externally connected ferroelectric capacitor (stacked with different FE materials). It is found that for the increased t_{fe}, the PVDF and $HfSiO_4$ exhibit superior performance for the above-mentioned insights. Secondly, the impact of the process variations with respect to the t_{fe} is analyzed and the variability in I_{ON}, SS, DIBL and temperature

Fig. 4 — Variability in ION, SS-DIBL with individual variation in (a – c) d, (d – f) S, (g - i) EOT, (j - l) W and (m - o) L_G for the t_{fe} ranging from (600-1000) nm.

effects is explored. The NC-CNFET based ring oscillator circuit produces reduced delay and shows excellent switching characteristics at low supply voltage of 75 mV.

Acknowledgements

The financial support of this work was given by the College of Engineering Guindy, Anna University, Chennai, India (Grant No. Lr. No. CFR/ACRF/2016/20).

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