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Design and performance analysis of a new efficient coplanar quantum-dot cellular automata adder

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Quantum-dot cellular automata (QCA) nanotechnology has the potential for revolutionizing the way computers are used. QCA computing has numerous advantages of ultra-low energy dissipation, improved performance and high device density. An adder is the most elementary component in arithmetic units of processors. Lot of work has been in progress to design and implement efficient adder circuits in QCA nanotechnology. This paper presents design and performance analysis of a new efficient coplanar adder in QCA nanotechnology. The proposed adder design uses 20% less QCA cells as compared to previous similar design due to better arrangement of QCA cells in the layout and has a delay of 1 clock cycle with an area of 0.04 μm^2. The proposed adder has 19% less average leakage energy dissipation, 28% less average switching energy dissipation, and 25% less average energy dissipation than the best reported previous coplanar adder design. The cost function of proposed efficient adder is equal to best reported previous coplanar adder.

Keywords: Quantum cellular automata (QCA), Majority gate, Coplanar, QCA designer, QCA pro, Cost function

1 Introduction

Present CMOS technology has been facing several technological and fundamental challenges. This has slowed down the pace of CMOS technology and researchers are exploring alternate viable technologies those can replace CMOS in future circuits and systems[1]. Nanocomputing in broader sense refers to computing systems realized from nanoscale devices. Current nanocomputing research covers the study of novel nanoscale devices, quantum dots, heterostructures, carbon nanotubes, single electron structures and various molecules. These devices and structures exhibit quantum mechanical nature of the electrons. QCA has been identified as one of the key technologies for future computing applications. QCA is an emerging nanocomputing model that encodes, processes, and transfers digital information in a new way. QCA nanotechnology adopts transistor-less approach and employs arrays of QCA cells interacting among themselves by Coulombic repulsion over large arrays. The alignment of electrons at the edges provides the computational output. An external clock signal controls the alignment and the QCA circuits operate on the principle of Boolean logic[2].

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R Feynman, a Nobel laureate on December 29th 1959, delivered an excellent talk entitled "There's plenty of room at the bottom: an invitation to enter a new field of physics" on miniaturization to nanoscale. This opened multitude of new opportunities in this field[3]. G Bourianoff reviewed developments in the silicon industry over the past few decades to identify need of emerging nanoscale technologies. He categorized the devices, architectures, variables, and data representations that fall in this new space of emerging nanoscale technologies[4]. T V Gopal discussed trends, directions and applications in the field of nanocomputing[5]. Lent *et al.* from Notre Dame University in 1993 proposed a new paradigm called Quantum-dot Cellular Automata (QCA), a new nanostructure comprising of quantum-dots. QCA computing paradigm can process binary data at very high speed with extremely small power consumption[6]. Walus *et al.* have developed a design tool and explored it for QCA nanotechnology. They emphasized the need to develop new design and simulation tools to explore new emerging QCA based circuits and architectures[7-8]. Vankamamidi *et al.*[9] introduced techniques for clocking of the QCA circuits and systems. The critical path length in each clocking zone is reduced utilizing 2D techniques. Srivastava *et al.*

introduced the model for energy dissipation in QCA circuits[10] and a power estimation tool QCA Pro[11].

2 Quantum-Dot Cellular Automata (QCA)

Quantum dots are minuscule nanostructures arranged in arrays for meaningful computation. QCA architecture exploits arrangement of individual electrons that interact by Coulombic repulsion. This brought a major change in information processing way from the prevailing transistor based current switching circuits and systems. QCA approach implement a smart binary information processing method suitable for nanostructures. This new approach overcame limitations of transistor based circuits and systems. The polarization of QCA cell represents the binary information stored in the arrays of QCA cells. Polarization is the extent to which electronic charges align along the two cell diagonals. The standard solid state QCA cell has a cell height and width of 18 nm and quantum-dot diameter[12] of 5 nm. Figure 1(a) shows a typical quantum cellular automata (QCA) cell. Two electrons within a cell can tunnel amongst the four quantum-dots and no tunneling is permissible between nearby cells. The physical mechanism responsible for interactions within a cell is quantum-mechanical tunneling. At nanoscale the electron wave function starts leaking out of the restricting potential of a dot. The rate of this leaking can be restricted by having optimal spacing between quantum-dots of a cell during fabrication[13-14]. The quantum dots in a square QCA cell are assigned slot numbers clockwise from the dot 1 to 4 shown in Fig. 1(a). Figure 1(b) and (c) shows cell representing binary state '1' and '0', respectively. The two states in which electrons are in position '1' and '3' and '2' and '4' represent two stable ground states. These states are used for meaningful computations in digital circuits.

2.1 QCA nanostructures

The two anti-podal stable ground states in a QCA cell are used to characterize two logic levels in digital circuits. Figure 2(a) shows a typical QCA binary wire realization[15-16]. The polarization of input QCA cell is fixed and it propagates to output QCA cell through Coulombic interactions occurring between nearby cells in the array, thus realizing a binary wire. There is no flow of electric charge when information propagates from input to output; only electronic polarization propagates towards output resulting in extremely low power dissipation. Figure 2(b) and (c) represents two different inverter realizations. Figure 2 (d) depicts a 3-input majority gate. It is the most fundamental device structure used in QCA circuits and systems. The middle cell is called decision cell and it is surrounded by 3 fixed inputs, labeled as input

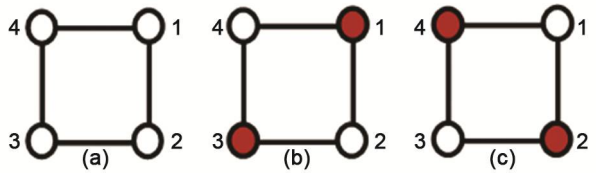

Fig. 1 – (a) Basic four-dot cell, (b) Binary logic '1' encoding, and (c) Binary logic '0' encoding

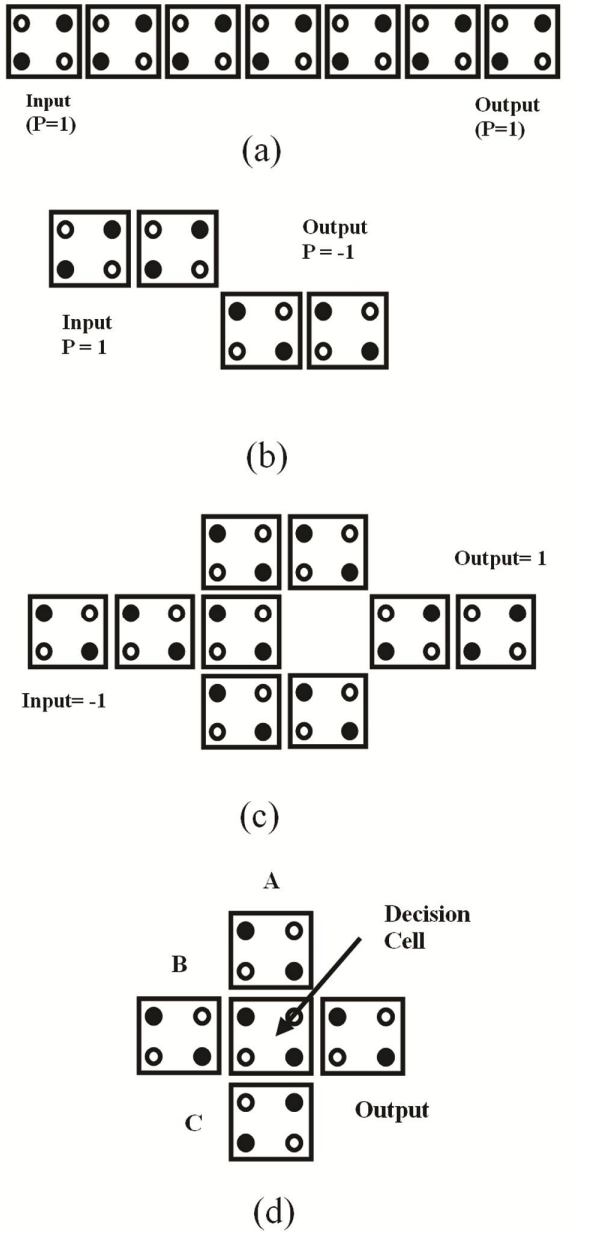

Fig. 2 – (*a*) a QCA binary wire, (*b*) an inverter (c) an alternate inverter configuration, and (d) Majority Gate[7]

A, input B, input C and one output. The decision cell acquires polarization according to polarization of majority of inputs. The output cell may drive other cells or wires. The majority gate can also function as programmable 'AND' and 'OR' gates provided one of its inputs is set at polarization state '-1' or '1'. So, any Boolean function can be realized in QCA logic using majority gates and inverters.

2.2 Cell-cell response

The polarization of an isolated cell is different and adjusts if it is encircled by other cells. Figure 3 illustrates that polarization of a cell 1 (P1) is influenced by polarization of its nearby cell (P2). If there is a minute variation in polarization of cell 2, it may result in complete change in polarization of cell 1 by dynamically preferring one arrangement above the other. The steepness of polarization response curve is determined by the ratio of the quantum tunneling energy to the Coulombic energy for electrons on nearby sites. Presence of Coulomb repulsion within a cell tends to keep electrons apart. A careful design of cells must have strong nonlinear coupling characteristics. This response curve has two bistable states which forms the basis for digital computation. The nonlinear saturation is basically equivalent to gain facilitating in refurbishing signal levels stage after stage. The major advantage is that no power dissipation is involved when switching takes place from one state to another[17-18].

2.3 QCA clocking

The clock signal in QCA circuits plays a vital role in realizing timing. The layout of QCA cells in a circuit is partitioned into different clock zones. During clocking each zone is provided with a particular phase. A QCA cell experiences four clock zones- clock 0, clock 1, clock 2 and clock 3. Each clock zone has four different phases labeled as Switch, Hold, Release, and Relax. There is a phase shift of 90° between four successive phases of a clock zone. Figure 4 elaborates four phase switching realized in each clocking phases in different clock zones. The cells are unpolarized initially and inter-dot potential barriers are in low state before switching phase. The QCA cells start unpolarizing and their inter-dot potential barriers are low in switch phase. Then the inter-dot barriers are gradually raised and the electrons transfer amongst the quantum-dots in a cell starts and the QCA cells assume one of two ground state polarization states, i.e., either P =1 or P = –1 according to state of their input cells[9,18-19]. The inter-dot tunneling barriers become high at the end of switch phase. In the hold phase, high state of tunneling barriers is maintained. During release phase, inter-dot tunneling barriers are lowered and QCA cells are allowed to become unpolarized. In relax clock phase, inter-dot tunneling barriers remain lowered and QCA cells are in an unpolarized state. Information transfers in a pipelined manner from inputs towards outputs during four clock zones.

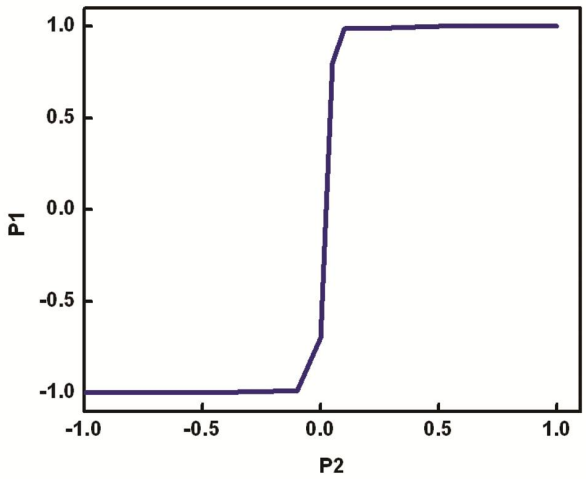

Fig. 3 – The cell-cell response curve[7]

3 Evolution of QCA Adders

One of the most basic components in arithmetic units is the full adder (FA). So, design of a robust adder in QCA technology is basic necessity for a high

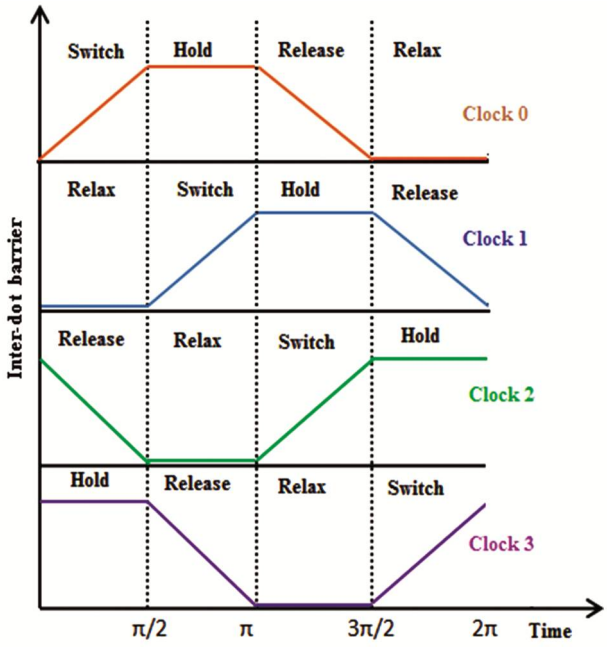

Fig. 4 – Clocking phases in different clock zones[15]

performance arithmetic unit. Lot of research work has been going on towards design of structurally robust and efficient QCA adders. Broadly, depending on wire crossing method QCA adders are classified into two categories- coplanar and multi-layer. In coplanar adders all QCA cells are arranged in the same plane, whereas in multi-layer adders QCA cells are arranged in different planes. Tougaw and Lent proposed first QCA-based 1-bit full adder (FA) design comprising of five majority gates, three inverters, and 9 wire crossovers. It utilizes 192 QCA cells. Another QCA FA proposed by Wang *et al.* comprises of three majority gates and two inverters, 6 wire crossovers and utilizes only 145 QCA cells[20]. Hänninen *et al.* proposed a new QCA adder layout comprising of three majority gates and two inverters, 3 wire crossovers and utilizes only 102 QCA cells[21]. Abedi *et al.* introduced a new coplanar adder design that uses clock-zone based technique to eliminate wire cross-over problem. It comprises of three majority gates and two inverters, and utilizes only 59 QCA cells with no wire crossovers[22]. Apart from coplanar adders, new QCA adder designs, multi-layer adder designs, and fault-tolerance in adders have been presented by many researchers[23-31]. The major advantages offered by multi-layer adder deign are the reduced complexity and delay. However, multi-layer designs impose several fabrication related constraints. The fabrication cost for a multi-layer design is considered to be 3 times than that of a coplanar design.

4 Proposed Coplanar QCA Adder Design

A new highly area efficient coplanar QCA adder design is proposed in this section. The schematic of the proposed coplanar adder is shown in Fig. 5. It comprises of 3 majority gates and two inverters with no wire crossing. The proposed QCA adder uses only 47 QCA cells and area efficient as compared to other coplanar adders reported in literature. This new design has latency of only 1 clock cycle. Figure 6 shows QCA implementation of the proposed coplanar QCA adder. Table 1 shows comparison of coplanar QCA full adders in terms of performance metrics-number of majority gates, number of inverters, number of wire-crossings, delay, and QCA cells. It is evident that proposed coplanar QCA adder employs same number of majority gates and inverters as reported in best coplanar QCA adder[30] with no wire-crossing and delay of 1 clock cycle. Also the proposed adder design uses 20% less QCA cells due to better arrangement of QCA cells in the layout. It also avoids use of clock-zone based technique to eliminate wire cross-over problem as optimization of delay of a complex QCA circuits becomes very tedious task.

5 Simulation Results

The functional verification of the proposed design as well as of previous coplanar full adder designs reported in literature has been performed using QCA designer version 2.0.3 tool. The coherence vector simulation parameters used are: cell width =18 nm, cell height =18 nm, dot diameter =5 nm, relaxation time $=1\times10^{-15}$ s, time-step $=0.1\times10^{-15}$ s, total

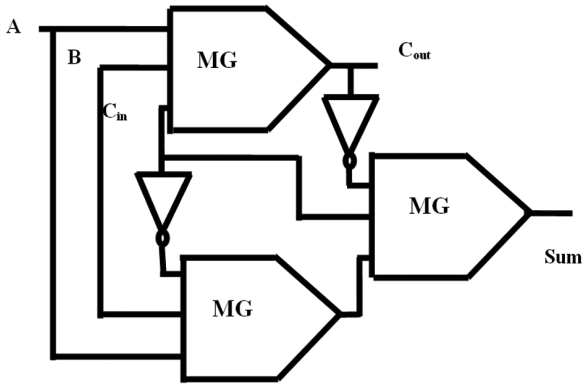

Fig. 5 – Schematic design of proposed coplanar adder

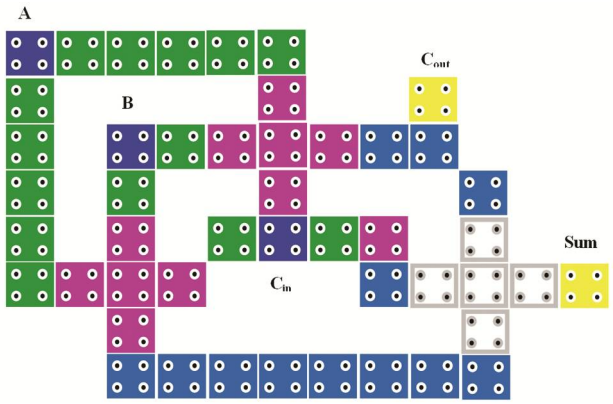

Fig. 6 – QCA implementation of proposed coplanar adder

Table 1 – Comparison of coplanar QCA full adders

Coplanar adders	Number of majority gates	Number of inverters	Number of wire-crossings	Delay (Cycles)	Number of QCA cells
Tougaw[12]	5	3	9	1.25	192
Wang[20]	3	2	6	1.25	145
Hänninen[21]	3	2	3	2	102
Abedi[22]	3	2	0	1	59
Proposed adder	3	2	0	1	47

simulation time =7.0×10^{-11} s, , clock high =9.8×10^{-22} J, clock low = 3.8×10^{-23} J, clock shift =0, clock amplitude factor =2.0, radius of effect = 80.0 nm, relative permittivity =12.9, and layer separation =11.5 nm. Figure 7 presents the simulation waveforms for the proposed coplanar full adder design. The output 'Sum' is high when inputs (ABC_{in}) are '001', '010', '100', and '111'. Similarly output carry 'C_{out}' is high when inputs (ABC_{in}) are '011', '101', '110', and '111'. As evident from simulation results, the output 'Sum' appears after a delay of 1 clock cycle and output carry 'C_{out}' after a delay of 0.75 clock cycles. An accurate power estimation tool QCA Pro has been used for energy dissipation results and generating thermal layout of the proposed adder design. Table 2 lists energy dissipation results of coplanar QCA full adders and Fig. 8 shows the bar-graph comparison of computed leakage energy dissipation, average switching energy dissipation, and average energy dissipation with reported QCA adder circuits. The results reveals that proposed adder design dissipate 28% less switching energy, 19% less average leakage energy and 25% less average energy as compared to previous best coplanar adder circuit at $1.0E_k$ tunneling energy level.

Figure 9(a) shows layout of polarization level of each cell in the proposed adder. The darker cells indicate higher levels of polarization. Figure 9(b) illustrates thermal layouts generated using QCA Pro tool for the proposed coplanar adder circuit. The dark cells in the circuit represent more average energy dissipation. The polarization level layout and thermal layout have been generated by simulating the proposed adder circuit considering all inputs from 000 to 111 for tunneling energy level of $1.0E_k$ and 2.0 K temperature.

A set of new cost functions has been proposed suitable for performance evaluation of QCA circuits[32].

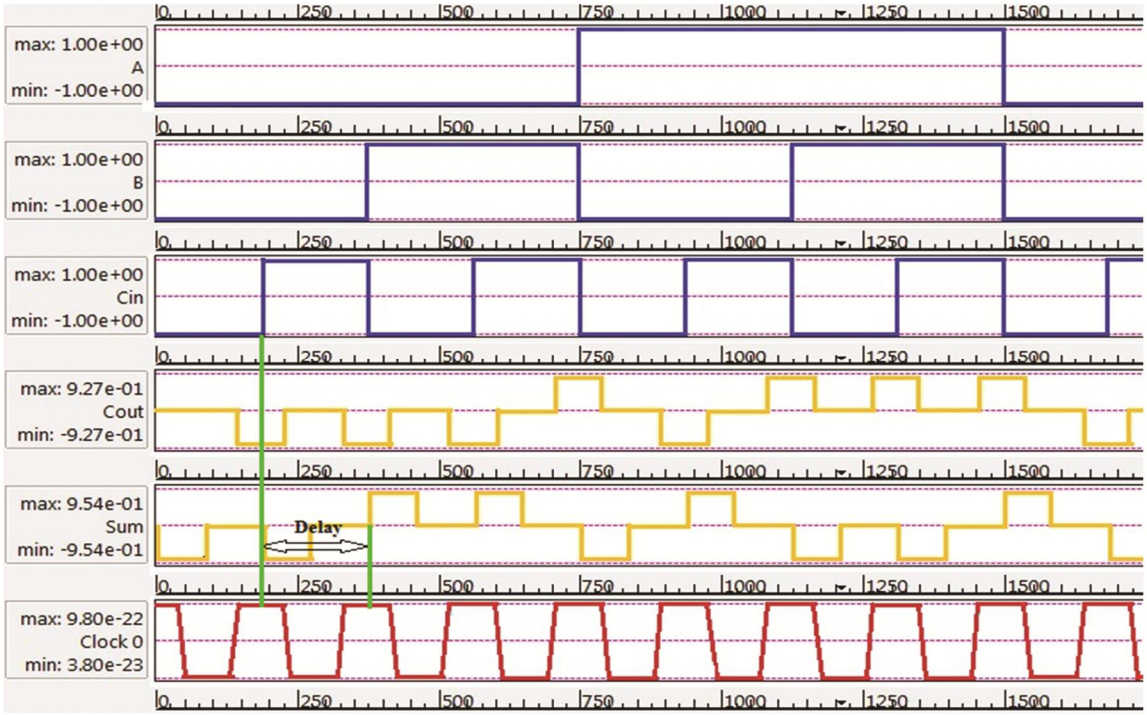

Fig. 7 – Simulation waveforms for the proposed coplanar adder design

Table 2 – Comparison of energy dissipation results of coplanar QCA full adders

Coplanar adders	Average leakage energy dissipation (meV)	Switching energy dissipation (meV)	Average energy dissipation (meV)
Tougaw[12]	313.84	233.3	547.16
Wang[20]	244.50	164.56	409.05
Hänninen[21]	160.06	87.89	247.95
Abedi[22]	51.41	90.92	142.33
Present study	41.68	65.17	106.86

The cost function can be computed by Eq. (2) as follows:

$$\text{Cost}_{QCA} = (M^k + I + C^l) \times T^p,\ 1 \le k, l, p \quad \ldots (1)$$

where, M, C, and I represent number of majority gates, number of wire crossovers, and inverters respectively. The term T represent delay of the circuit and k, l, p are exponential weightings for majority gate count, wire crossover count and delay.

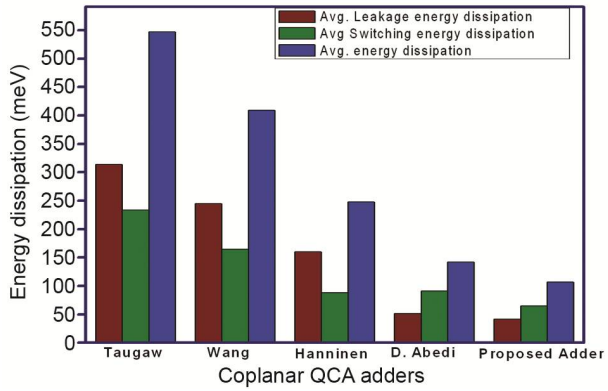

Fig. 8 – Bar-graph comparison of proposed adder design with previous reported designs

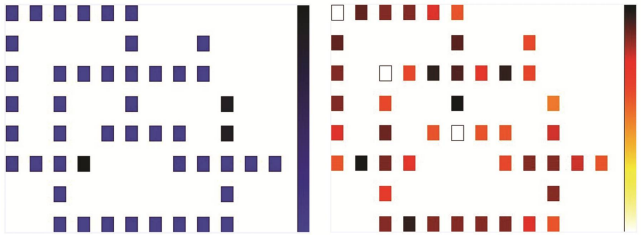

Fig. 9 – (a) Layout of polarization level of proposed adder design and (b) Thermal layout for average energy dissipated in each cell of proposed coplanar adder design

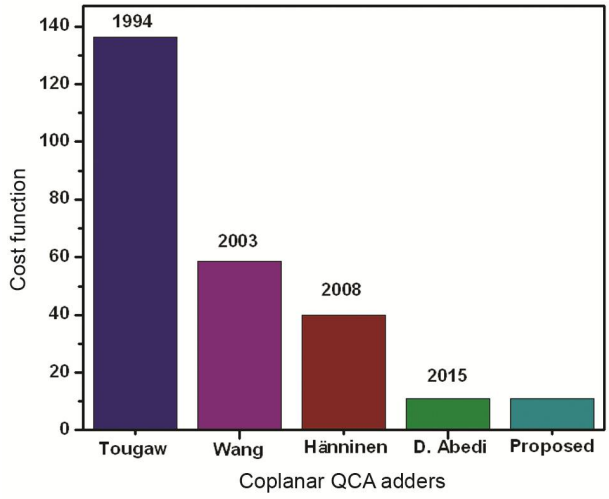

Fig. 10 – Cost function for coplanar adder designs

The cost functions provide different metrics in accordance with values assigned to k, l and p. The values assigned to k, l and p are decided according to the overall design optimization goal. The cost function have been evaluated for Taugaw[12], Wang[20], Hänninen[21], Abedi[22], and the proposed coplanar QCA adder circuits for generalized case of k=2, l=2, and p=1 as shown in Fig. 10. The Taugaw adder has highest cost function value, i.e., it is complex and poor in performance. The best reported Abedi QCA adder[22] and proposed adder have equal cost function value. It means the proposed coplanar adder is not complex and is better in performance.

6 Conclusions

This paper presents design and performance analysis of a new efficient coplanar QCA adder design. The proposed QCA adder design has been functionally verified using QCA designer tool and energy dissipation computations have been performed using QCAPro tool. The proposed adder design utilizes '3' three-input majority gates and two inverters only. It uses only 47 normal QCA cells with an area of 0.04 μm^2 and has delay of 1 clock cycle. It has 20% less QCA cells as compared to previous similar design due to better arrangement of QCA cells in the layout. The proposed adder circuit uses no wire cross-over. The proposed adder dissipates 19% less average leakage energy, 28% less average switching energy, and 25% less average energy than best reported previous coplanar adder design. It has cost function equal to best reported previous design.

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