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Realization of resistorless floating inductor using modified CDTA

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This paper briefly introduces a modified current differencing *trans*-conductance amplifier (M-CDTA) and its application in the simple realization of floating inductors. The proposed inductor is positive floating and lossless type offering the advantage of wider frequency bandwidth. The resulting equivalent inductance has been realized using one M-CDTA and one grounded capacitor and its inductance value can be adjusted electronically by proper tuning of the bias current. Results demonstrating the behavior of the circuit and its application confirming the theoretical analysis are verified through PSPICE simulations.

Keywords: M-CDTA, Electronically adjustable, Floating inductor, Resistorless, Grounded capacitor

1 Introduction

During the last two decade much effort has been applied in the realization of inductor as it is one of the very important element in the design of filter and oscillator. The large size of the available coil inductor makes it impossible to fabricate on chip. Floating inductor simulator circuit offering high performance has been excavated and reported several times in the literature with a possible reason the emerging application[1-9]. The current-mode circuits have become a topic of keen interest because of their potential advantage in, simple circuitry, better linearity, reduced power consumption and increased dynamic range[10,11]. The circuit introduced in this paper offers considerable advantages such as compact structure, and a circuit design which is resistorless.

CDTA is a 5-terminal current mode active element[12], and it is found to be a versatile element in the realization of filters used in analog signal processing circuits. It offers wider frequency bandwidth and it is free from parasitic input capacitances.

This paper aims to introduce a modified version of CDTA and its application in the realization of inductor. The proposed lossless inductor is resistorless and it is electronically tunable by adjusting the bias current.

2 Circuit Configuration

2.1 Basic concept of M-CDTA

The proposed M-CDTA is similar to that of conventional CDTA with the exception of an OTA preceding CDTA offering non-zero input voltage at the *p* and *n* input terminals, respectively. The symbol of M-CDTA is illustrated in Fig. 1.

From the basic operation of ideal M-CDTA, the relationship between its terminals can be characterized by the help of following matrix:

$$\begin{bmatrix} I_z \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & g_{m1} & -g_{m1} \\ g_{m2} & 0 & 0 \\ -g_{m2} & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ V_p \\ V_n \end{bmatrix} \quad \ldots (1)$$

where g_{m1} and g_{m2} are the *trans*-conductance gain of OTA and CDTA, respectively. Here g_m depends on external DC bias current, and hence the proposed configuration is electronically tunable.

2.2 Inductance simulator using M-CDTA and a grounded capacitor

A positive lossless floating inductor can be realized by the help of one M-CDTA and a grounded capacitor as shown in Fig. 2

Analyzing the proposed floating inductor yielded the following relation:

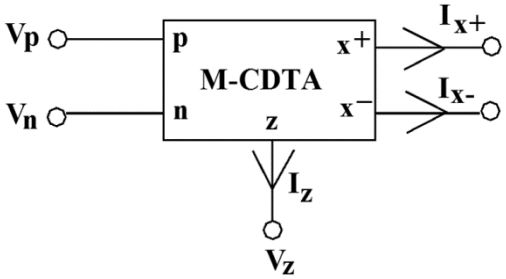

Fig. 1 – Symbol of M-CDTA.

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$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = [Y_{eq}] \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad \text{... (2)}$$

$$Y_{eq} = \left(\frac{2g_{m1}\, g_{m2}}{SC}\right) \quad \text{...(3)}$$

$$Z_{eq} = \frac{1}{Y_{eq}} = s\left(\frac{C}{2g_{m1}g_{m2}}\right). \quad \text{...(3.1)}$$

$$Z_{eq} = sL_{eq} \quad \text{...(3.2)}$$

Where C is a grounded capacitor. It is very much evident from Eq. (3) that the equivalent value of the realized floating inductance is found to be:

$$L_{eq} = \frac{C}{2g_{m1}\, g_{m2}} \quad \text{...(4)}$$

Obviously L_{eq} is electronically tunable, lossless and resistorless.

The floating inductor circuit realized in Fig. 2 is using the following components: C= 1 nF, $g_m = g_{m1} = g_{m2}$ = 427.599 µA /V, which results in L_{eq} = 2.73 mH.

3 Applications

3.1 Application of floating inductance simulator as a band pass filter

Application of the proposed floating inductor in Fig. 2 can be demonstrated by employing in a RLC band pass filter as shown in Fig. 3.

The transfer function obtained from Fig. 3 is given as:

$$\frac{V_0}{V_{in}} = \frac{S\left(\frac{2Rg_{m_1}g_{m_2}}{C}\right)}{S^2 + S\left(\frac{2Rg_{m1}\, g_{m2}}{C}\right) + \frac{2g_{m1}\, g_{m2}}{C^2}}$$

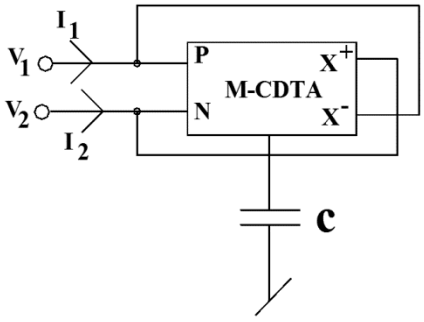


Fig. 2 – Inductance simulator.

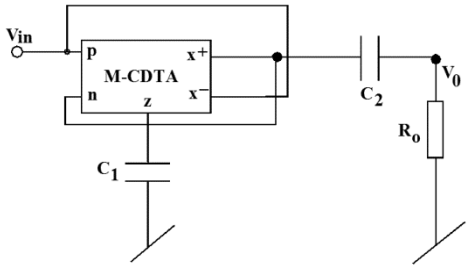


Fig. 3 – BPF based on inductor simulated using M-CDTA.

$$\omega_0 = \frac{1}{C}\sqrt{2g_{m1}g_{m2}}$$

$$Q_0 = \frac{\omega_0\, C}{2Rg_m^2}$$

$$f_0 = \frac{1}{2\pi C}\sqrt{2g_{m1}g_{m2}}$$

The components specifications used are C=1 nF, R = 2.338 kΩ, $g_{m1} = g_{m2}$ = 427.99 µA/V, it is observed that the frequency was found to be 96.3 KHz.

3.2 Application of floating inductance simulator as normalized fourth order butterworth LPF

To demonstrate the application of the proposed floating inductor in Fig. 2, it is also employed in a normalized fourth order butterworth LPF as shown in Fig. 4.

4 Simulation Results

The theoretical predictions of the proposed inductance simulator, the band pass filter and fourth order butterworth LPF employing M-CDTA have been verified in this section using PSPICE program and are shown in Fig. 5, Fig. 6 and Fig. 7, respectively. The CDTA was realized using 0.50-µm CMOS technology. For all inductor and filter response value of capacitor is taken as 1 nF and *trans*-conductance gain is set around 427.599 µA/V (which is obtained from OTA structure[26] of Fig. 4). Extremely little deviation is observed in the ideal and the simulated value of inductor as well as the cut-off frequency of band pass filter. L_{eq} (simulated)

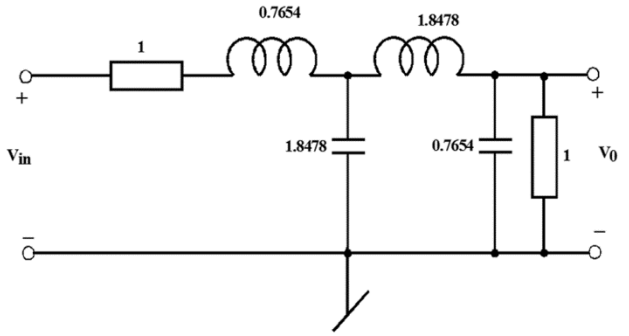


Fig. 4 – Normalized fourth order Butterworth LPF.

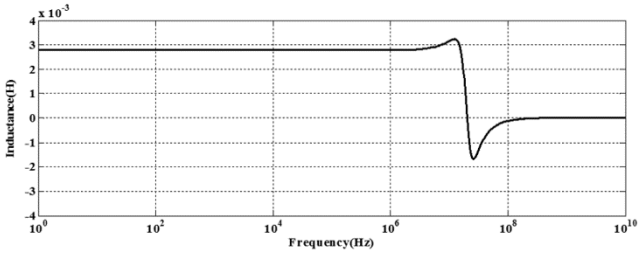


Fig. 5 – Frequency response of the simulated floating inductor.

= 2.789 mH and f_0 (simulated) = 95.641 kH. The comparison of the proposed circuit with other published work is shown in Table 1.

The transfer function obtained from Fig. (8) is given as:

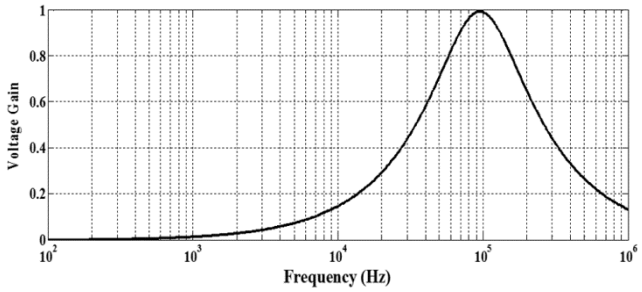


Fig. 6 – Frequency response of BPF using the simulated floating inductor.

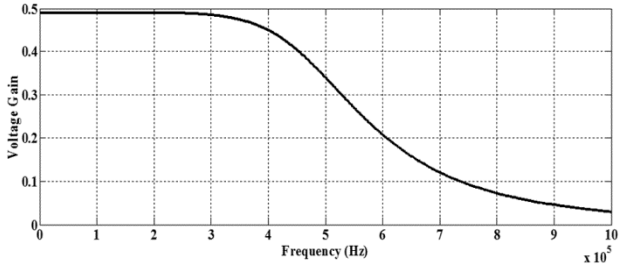
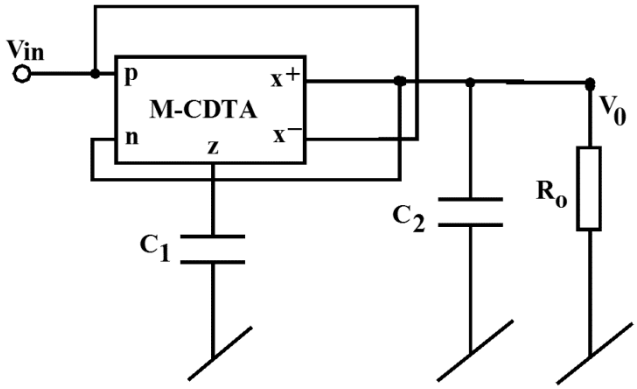


Fig. 7 – Frequency response of fourth order Butterworth LPF.



$$\frac{V_0}{V_{in}} = \frac{s^2}{s^2 + s\left(\frac{2g_{m1}\,g_{m2}}{C_1}\right) + \frac{2g_{m1}\,g_{m2}}{C_1 C_2}}$$

Fig. 8 – HPF based on the proposed inductor.

5 Conclusions

This paper presents a compact configuration of modified CDTA (M-CDTA) and its application as the realization of floating inductance simulator, band pass filter and normalized fourth order butterworth low pass filter. The inductance simulated has several advantages such as: 1) only one passive component, i.e., a grounded capacitor is used; 2) no matching constraints (lossless); 3) electronically controllable

Table 1 – A table of comparison with few existing floating inductors available in literature.

References	Number of active building blocks	Number of passive elements	Technology used	Tunability	Type of capacitor used (F-floating G-grounded)	Matching conditions
[2]	2	3	0.35 µm /MOS	None	F	Yes
[3]	3	1	MOS	None	G	No
[5]	≥2	≥3	0.35 µm /MOS	None	G	Yes
[6]	2	3	0.35 µm /MOS	Resistor	G	No
[7]	2	3	0.35 µm /MOS	None	G	Yes
[8]	2	3	0.25 µm /MOS	Current	G	No
[9]	1	3	0.35 µm /MOS	None	G	No
[13]	2	3	0.25 µm /MOS	None	G	No
[14]	≥3	4	BJT	None	G	No
[15]	1	4	0.18 µm /MOS	None	F	Yes
[16]	2	1	BJT	Current	G	No
[17]	4	4	MOS	Voltage	G	No
[18]	3	1	0.35 µm /MOS	Current	G	No
[19]	3	1	BJT	None	G	No
[20]	2	2	0.25 µm /MOS	Current	G	No
[21]	3	1	BJT	Current	G	No
[22]	2	3	0.18 µm /MOS	None	G	No
[23]	1	2	0.5 µm /MOS	Current	G	No
[24]	2	3	0.13 µm /MOS	None	G	No
[25]	1	2	0.18 µm /MOS	Current	G	No
Proposed	1	1	0.5 µm /MOS	Current	G	No

using bias current; 4) low sensitivity. The SPICE simulations results are also included to justify the work proposed here.

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