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Thermal stability analysis and performance exploration of asymmetrical dual-k underlap spacer (ADKUS) SOI FinFET for high performance circuit applications

Neeraj Jain & Balwinder Raj*

Department of Electronics and Communication Engineering,
Dr B R Ambedkar National Institute of Technology (NIT), Jalandhar 144 011, India

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This paper explores the performance of asymmetrical dual-k underlap spacer (ADKUS) SOI FinFET (device-D1) over the wide temperature range (200 K-450 K). An attempt has been made to find out the zero temperature coefficient (ZTC) biased point to enhance the digital, analog and RF performance at 20 nm channel length. The proposed device will be suitable for VLSI circuit's design, internet of things (IoT) interfacing components and algorithm development for security applications of information technology. The potential parameters of device-D1 like intrinsic gain (A_V), output conductance (g_d), transconductance (g_m), early voltage (V_{EA}), off current (I_{off}) , on current (I_{on}), I_{on}/I_{off} ratio, gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}), cut-off frequency (f_T), energy (CV^2), intrinsic delay (CV/I), energy-delay product (EDP), power dissipation (PD), sub-threshold slope (SS), Q-Factor ($g_{m,max}$/SS), threshold voltage (V_{th}) and maximum trans-conductance ($g_{m,max}$) are subjected to analyze for evaluating the performance of ADKUS SOI FinFET for wide temperature environment. The validation of a temperature based performance of ADKUS SOI FinFET gives an opportunity to design the numerous analog and digital components of internet security infrastructure at wide temperature environment. These ADKUS SOI FinFET based components give new technology to the IoT which has the ability to connect the real world with the digital world and enables the people and machines to know the status of thousands of components simultaneously.

Keywords: ADKUS SOI FinFET, CMOS, Transconductance, Analog/RF performance, Intrinsic gain, Temperature, Capacitance

1 Introduction

Today requirement of low power and high-performance devices in the consumer products has become the driving force to develop the new technology in the semiconductor industries. The invention of FinFET greatly enables the development of complex integrated circuits for a variety of applications due to its 3-D(dimensional) quasi-planar geometry[1]. The developments in semiconductor devices are bringing improvements in VLSI circuits design, internet infrastructure and algorithms for security and privacy applications of information technology[2]. FinFET is one of the most desirable multi-gate structure in CMOS technology due to its high immunity to short channel effects (SCE's), excellent scalability and very close to MOSFET in respect to layout design[3]. The analog components based on FinFET technology used in sensors (temperature, motion, pressure, shock, proximity, sound, gas, infrared, etc.), amplifiers, signal processors, microcontroller and integrated chips give better technology to the internet of things (IoT) applications[4–7]. Therefore, world top semiconductor leading industries like TSMC and Cadence designed the FinFETs at 7 nm technology node for security and high-performance computing platforms and others companies are further trying to improve the performance of FinFET by optimizing the underlap spacer region at lower technology nodes[8,9]. However, there is always a tradeoff among SCEs and analog/RF performance of FinFET. Further, improvement in FinFET structure has been done through SOI layer, high-k spacer and source/drain engineering techniques[10,11]. As per demand for variety of applications in the semiconductor industries, a lot of advanced device structures proposed in literature like pi-gate[12,13], ohm-gate[14], tri-gate, planar double gate SOI MOSFETs, Bulk FinFETs, SOI FinFETs and all around gate[15–19]. According to literature, significant work already proposed with dual-k and high-k spacers to improve the SCEs and analog/RF performances of underlap SOI FinFETs [20,21]. Similarly**,** Pal *et al.*[9,22] demonstrate the asymmetric dual-k spacers and symmetrical SOI FinFET structures for a high-performance application. Goel *et al.*[23,24] also

*Corresponding author (E-mail: balwinderraj@gmail.com)

elaborated the asymmetrical dual-k spacer SOI FinFET structure for low power and digital SRAM applications. Beside these, some applications like automobiles, military and nuclear sectors require high temperature operated integrated circuits (ICs) and other like medical diagnostic systems and space applications require low temperature based operated equipment. Some industries demand both high and low-temperature sustainable ICs for their application. FinFETs are the devices which fulfill the requirement of these ICs and chip industries are now trying to implement the FinFET circuits in all electronic gadgets like computer chips, mobile phones and sensor-based high performance security and privacy systems.

This work demonstrates the effect of dual-k underlap spacer at the drain side on the analog/RF performance of ADKUS SOI FinFET and investigation is done for the ZTC point over the wide temperature range. As compared to conventional bulk FinFET this architecture enhances the analog and RF performance of complex integrated circuits without increasing the effective chip area. The ADKUS SOI FinFET device with combination of dual- k spacers (inner underlap side of gate high-k (HfO_2) and outer side the low-k (Si_3N_4)) at the drain side is explored for wide temperature range. The performance of ADKUS SOI FinFET is analyzed in terms of analog/RF performance parameters like I_{on}, I_{off}, I_{on}/I_{off}, output conductance (g_d), transconductance (g_m), transconductance generation factor (TGF), sub-threshold slope (SS), intrinsic gain (A_V), early voltage (V_{EA}), gate capacitance (C_{gg}), gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}) and cut-off frequency (f_T) etc.

The sensitivity of ADKUS SOI FinFET in the temperature range 200 K-400 K towards analog/RF design is very crucial and the investigation is done for ZTC bias point using 3D simulations process. ZTC bias point is an important parameter which describes the stability of semiconductor device and shows the negligible variation in current-voltage (*I-V*) characteristic with temperature. The previous literature works by Mohapatra *et al.*[25] and Sahu *et al.*[26] have been done with ZTC bias point for MOSFETs stability analysis. In this paper, demonstration of ADKUS SOI FinFET for stability analysis has been done by ZTC bias point over the wide temperature range (200 K- 450 K). As compared to MOSFET, SOI FinFET gives better temperature performance at sub-20 nm technology node.

2 Structures and Simulation Setup

Schematic diagram of asymmetrical dual-k underlap spacer (ADKUS) SOI FinFET structure is shown in Fig. 1(a). For this FinFET structure, 20 nm channel length is considered for 3D- simulations. Source/drain part of ADKUS SOI FinFET structure is heavily doped as n-type 1×10^{20} cm^{-3} and the channel region of the FinFET structure is lightly doped as p-type 1×10^{15} cm^{-3}. Source/drain is heavily doped to overcome the effect of mobility degradation which is the effect of coulomb charge scattering. Here the total effective width of FinFET device $W=\left(2H_{Fin}+W_{Fin}\right)$ is considered because the total current of the FinFET structure at sub-20 nm technology node is the effective sum of all current components flowing along the sidewalls and the top surfaces of Fin[27]. Metal gate technology is used in ADKUS SOI FinFET structure because it eliminates the poly gate depletion effect in all semiconductor devices. The length of source /drain is fixed to 40 nm with vertically placed source and

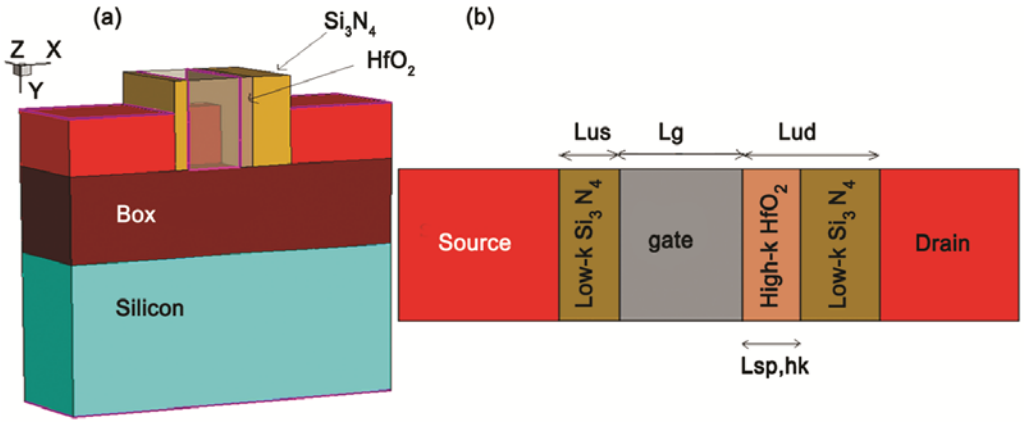

Fig. 1 – (a) Asymmetrical dual-k underlap spacer SOI FinFET (device-D1) and (b) cross-section view of device D.

drain contacts, respectively. Device dimensional parameters of ADKUS SOI FinFET device used for 3D simulation in this paper are given in Table 1.

Figure 1(b) shows the cross-section view of ADKUS SOI FinFET structure in which dual-k spacer is used for underlap region at the drain side. Underlap region (Lud) which is a combination of two high-k (gate side, Lsp, hk) and low-k (drain side, Lsp, lk) materials. At the source side low-k (Si_3N_4) spacer material is used. The high-k spacer is used to increase the I_{on} current of FinFET by optimizing the gate induced barrier lowering (GIBL) while the low-k spacer is used to optimize the effect of parasitic extrinsic capacitances. In conventional FinFETs, the high-k spacer at the drain side improves the driving current with a significant reduction of off-state leakage current. However, these devices suffer by increased total effective gate fringing capacitances which results in poor device cut-off frequency (f_T) and circuit level delay[28]. So dual-k spacer is used to get optimum analog and RF performance at lower technology node. A substrate with a lightly doped concentration of 1×10^{15} cm^{-3} is used to minimize the effect of random dopants fluctuations in ADKUS SOI FinFETs for performances analysis[29].

The underlap region in SOI FinFET increases the distributed channel resistance or degradation in I_{on} current and faces the problem of controlling the doping profile. However, these problems are well tackled in literature[30–32]. The asymmetric underlap region at drain side for MOSFETs and degradation in I_{on} can be improved further by introducing inner high-k spacer in underlap region without any significant degradation of output fringing capacitance[33].

The ADKUS SOI FinFET structure follows the standard FinFET process flow[34]. In ADKUS SOI FinFET process flow, prior fabrication of source-drain lateral extension region, spacer regions are fabricated. Initially, the dual-k spacer region is engineered in the FinFET device and fabrication of dual-k region follows the two-step process. In first step formation of high-k spacer using selective epitaxial growth technique at the drain side followed by the second step in which low-k offset spacer is formed both at the source and drain side[35–37]. Low-k offset spacer at the drain side kept longer to ensure asymmetric underlap region during source/drain extension region fabrication by tilt ion implantation[38–40].

The 3-D simulations of ADKUS SOI FinFET structure are carried out using Sentaurus TCAD simulator tool[41]. Analog/RF performance of device D1 is explored at 200 K-450 K temperature range for total length[24] under drain side of 20 nm. The metal gate work function is set to 4.3 eV. The equivalent oxide thickness[42–44] (t_{0x}) is taken a value of 0.9 nm at the supply voltage V_{DD} of 0.7 *V* and other parameters considered according to International Technology Roadmap for Semiconductors[45] (ITRS-2013). The simulation validation of simulator is investigated by reported results in the previous literature data[44]. The models considered in this paper are velocity saturation model, concentration-dependent and field dependent mobility that consider the doping models[46]. The inversion mobility Lombardi CVT[47], models of auger recombination with Shockley –Read-Hall (SRH)[47–49], default carrier transport model and quantum confinement are also considered for simulation process. Junctions with smooth meshing and all biasing are done at a wide range of temperatures to evaluate the performance of ADKUS SOI FinFET structure.

3 Results and Discussion

In this section, the performance of ADKUS SOI FinFET (Device-D1) in terms of energy (CV^2), intrinsic delay (CV/I), energy-delay product (EDP), power dissipation (PD), sub-threshold slope (SS), Q-Factor ($g_{m,max}$/SS), threshold voltage (V_{th}), maximum trans-conductance (g_{max}), on current (I_{on}), off current

Table 1 – Dimensional values used for simulation in this paper.

Parameters	Descriptions	Device-D1
W_{Fin}	Fin width	10 nm
L_g	Gate channel length	20 nm
H_{Fin}	Fin height	26 nm
t_{ox}	Oxide thickness	0.9 nm
BOX	Thickness of buried oxide	40 nm
L	Total length of device	120 nm
Lus =Lsp,hk (HfO_2)+Lsp,lk (Si_3N_4)	Spacer length under source side	Lsp, hk=0 nm, Lsp, lk=5 nm
Lud =Lsp,hk (HfO_2)+Lsp,lk (Si_3N_4)	Spacer length under drain side	Lsp, hk=5 nm, Lsp, lk=15 nm
$W_{s/d}$	Source/drain width	40 nm

(I_{off}), I_{on}/I_{off} ratio and the analog/RF performance parameters like intrinsic gain (A_V), output conductance (g_d), transconductance (g_m), early voltage (V_{EA}), gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}), total gate capacitance (C_{gg}) and cut off frequency (f_T) are evaluated for various temperature range (200 K to 450 K) for the low and high value of drain to source voltages V_{DS}=0.05 V and V_{DS}=0.7 V, respectively. The temperature variation in the semiconductor device severely affects its electrical characteristics parameters like mobility, sub-threshold slope, threshold voltage, leakage current, power dissipation and intrinsic delay becomes the major concern in the scaled technology design.

Figure 2 shows some device scalability performance characteristics of ADKUS SOI FinFET like SS, I_{on}, $I_{off,}$ I_{on}/ I_{off} ratio with temperature variation at V_{DS}=0.05 V and V_{DS}= 0.7 V. It is noticed from the Fig. 2(a) that on increasing the temperature sub-threshold performance of device degraded due to the reduction of I_{on} current both at a low and high value of V_{DS}=0.05 V and V_{DS}=0.7 V, respectively. SS is an important parameter which describes the I_{off} leakage current and related with temperature[50] according to as follows:

$$SS(mV/decade) \approx 60mV\frac{T}{300K} \quad \ldots(1)$$

According to Eq. (1), at a low temperature range (below 250 K), there is much reduction of SS value that directly reflects the off state leakage current of the semiconductor device and improvement in I_{off} at lower temperature range is shown in Fig. 2(c). So, at low temperature (below 250 K), there is a noticeable improvement in I_{on}/I_{off} ratio due to a significant reduction of I_{off} current because of the low value of sub-threshold slope (SS) as shown in Fig. 2(d). The high value of I_{on}/I_{off} and low value of I_{off} is desirable for low power analog circuit applications.

The drain current (I_D) and transconductance (g_m) against gate-source voltage (V_{GS}) characteristics for various values of temperature range (200 K-450 K) at V_{DS}=0.05 V and V_{DS}= 0.7 V for ADKUS SOI FinFET are shown in Fig. 3(a) and (b), respectively. The drain

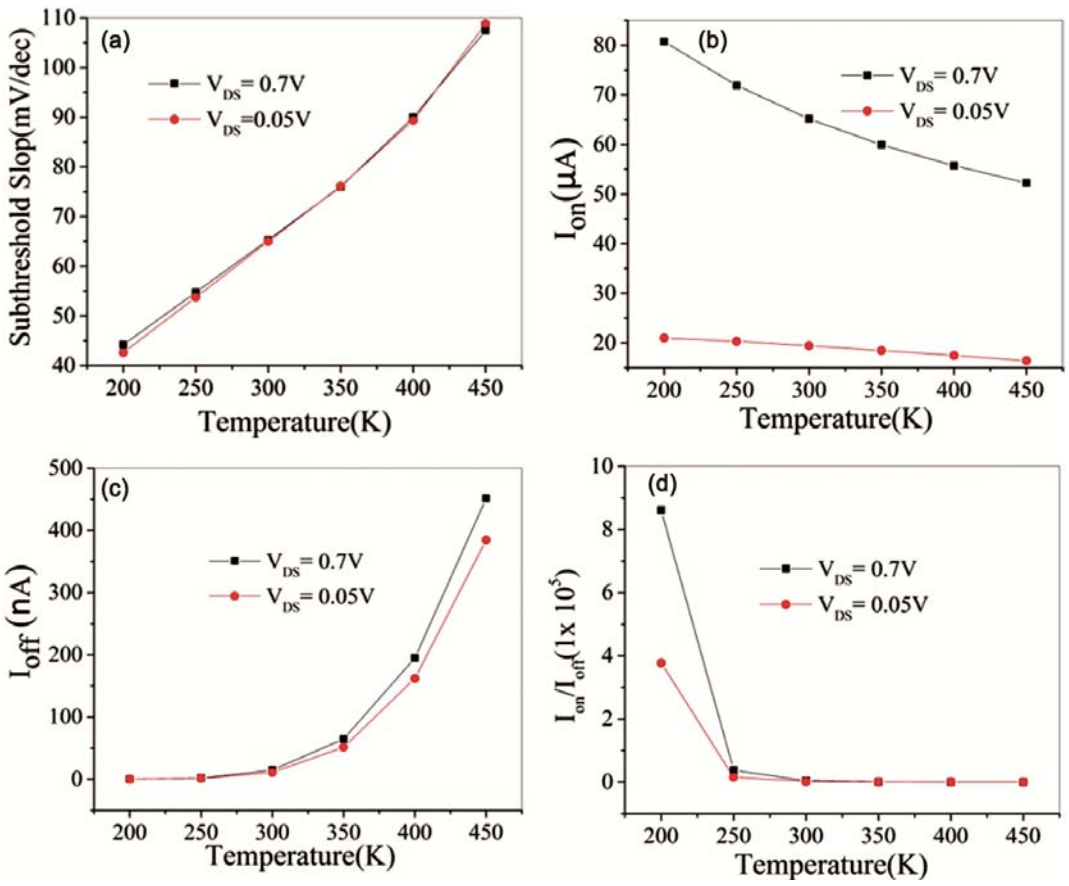

Fig. 2 – (a) Sub-threshold slope (SS), (b) on current (I_{on}), (c) off current (I_{off}) and (d) I_{on}/ I_{off} ratio versus temperature characteristics for ADKUS SOI FinFET at V_{DS}= 0.05 V and V_{DS}= 0.7 V.

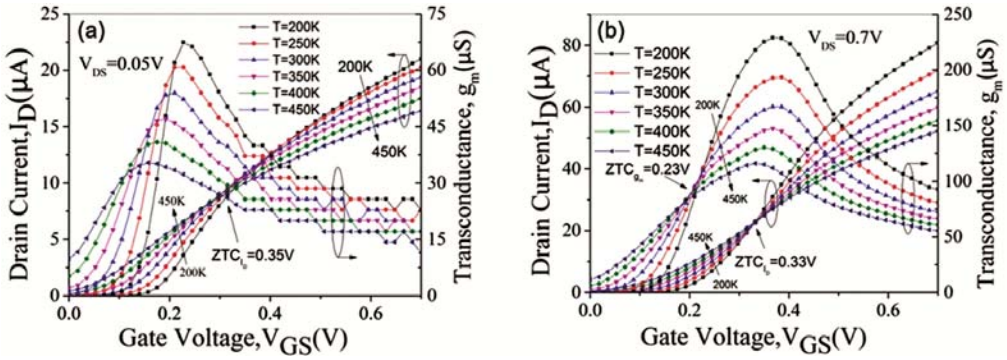

Fig. 3 – I_D and g_m versus V_{GS} characteristics of ADKUS SOI FinFET with temperature variation at (a) V_{DS}=0.05 V and (b) V_{DS}=0.7 V.

current as a function of mobility (μ) and threshold voltage[51] (V_{th}) is as follows:

$$I_D(T) \propto \mu(T)[V_{GS} - V_{th}(T)] \quad \ldots(2)$$

The mobility term and threshold voltage both are temperature dependent parameters. The carrier mobility follows the relationship as follows:

$$\mu(T) = \mu(T_0)(T/T_0)^{-n}$$

where n exponent[50] varies from 1.6 to 2.4.

The threshold voltage of SOI devices follows the inverse temperature characteristics and decreases with the increase of temperature[52]. On increasing the temperature, mobility of charge carrier also decreases for ADKUS SOI FinFET due to lattice scattering effects. So, $\mu(T)$ and $[V_{GS} - V_{th}(T)]$ terms of drain current shown in Eq. (2) will show the inverse nature with temperature variation. As increasing the temperature, $\mu(T)$ value decreases which tries to force drain current decrease while the value of $[V_{GS} - V_{th}(T)]$ term increases which tries to force drain current increases. So on increasing the gate bias point, these two effects compensated at a fixed value of gate to source voltage (V_{GS}) and effect of temperature variation at this point can be neglected for evaluating the performance of ADKUS SOI device. This gate bias point is known as zero temperature coefficients (ZTC) point.

As we observe from the I_D-V_{GS} characteristics shown in Fig. 3 that for low and high V_{DS} value below the ZTC_{I_D} point, drain current (I_D) increases with increasing the temperature while above the ZTC_{I_D} point nature of drain current becomes the opposite. As V_{GS}<V_{th}, current mainly flows by a diffusion process. So, below the ZTC_{I_D} point, $[V_{GS} - V_{th}(T)]$ becomes the dominating factor as compared to $\mu(T)$ due to more degradation of the threshold at a high value of temperature. So, drain current increases with the increase of temperature value. As V_{GS}>V_{th}, the dominating flow of current is by drift process. So, above the ZTC_{I_D} point, $\mu(T)$ decreases with the increase of temperature due to more lattice scattering effect and becomes the dominating factor for evaluating the drain current. So, drain current decreases with the increase of temperature value.

In Fig. 3(b), at V_{DS}= 0.7 V, we extract the two ZTC points for drain bias and trans-conductance bias ZTC_{I_D} and ZTC_{g_m}, respectively. Both these ZTC points are important figures of merit for analog circuit design at various temperature values. The ZTC_{I_D} bias point gives the information about constant DC current while ZTC_{g_m} bias point is used to achieve stable circuit parameters for analog design. Both bias points are affected by the process variation. So, ZTC points are chosen according to the applications. It is noticed from the Fig. 3(b) that the extracted value of $ZTC_{g_m} = 0.23V$ and $ZTC_{I_D} = 0.33V$ at V_{DS}=0.7 V. So, below 0.23 V the trans-conductance (g_m) increases due to degradation of V_{th} on increasing the temperature while above 0.23 V the g_m decreases due to the reduction of channel mobility by lattice scattering effects on increasing the temperature.

The output performance characteristics of ADKUS SOI FinFET, drain current (I_D) and output conductance (g_d) versus drain-source voltage (V_{DS}) at V_{GS}= 0.35 V and V_{GS}= 0.7 V are shown in Fig. 4 (a and b), respectively. From the Fig. 4(a and b), it is noticed that above the ZTC_{I_D} point, drain current decreases on increasing the temperature due to discussed $\mu(T)$ effect with temperature and opposite nature of current generated below the ZTC_{I_D}. The low

value of g_d is required to improve the intrinsic gain (g_m/g_d) of ADKUS SOI FinFET device. Further, g_d is less sensitive to temperature at V_{GS}= 0.35 V compare to V_{GS}= 0.7 V near the ZTC point of g_d and it can be analyzed from Fig. 4.

Figure 5 (a and b) and Fig. 6 (a and b) shows the gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) versus V_{GS} characteristics for ADKUS SOI FinFET at V_{DS}= 0.05 V and V_{DS}=0.7 V, respectively. From Fig. 5 (a) and (b), it is noticed that at V_{DS}=0.05V, ZTC for C_{gs} ($ZTC_{C_{gs}}$) has a value of 0.195 V without having the ZTC for C_{gd} (ZTC_{Cgd}). The C_{gs} increases with increasing the temperature below $ZTC_{C_{gs}}$ point whereas opposite nature of C_{gs} occurs above the $ZTC_{C_{gs}}$ point. In case of C_{gd}, it increases with gate bias in weak inversion region and has more value at high temperature after that it decreases in the strong inversion region with gate bias. It is noticed from the Fig. 6(a) that $ZTC_{C_{gs}}$ has the value of 0.3 V at V_{DS}=0.7 V and follow the same nature as at V_{DS}=0.05 V. In case of C_{gd}, two ZTC points generated at V_{DS}= 0.7 V due to dual-k spacer region at the drain side for ADKUS SOI FinFET. The variation of these two ZTC points is due to fringing

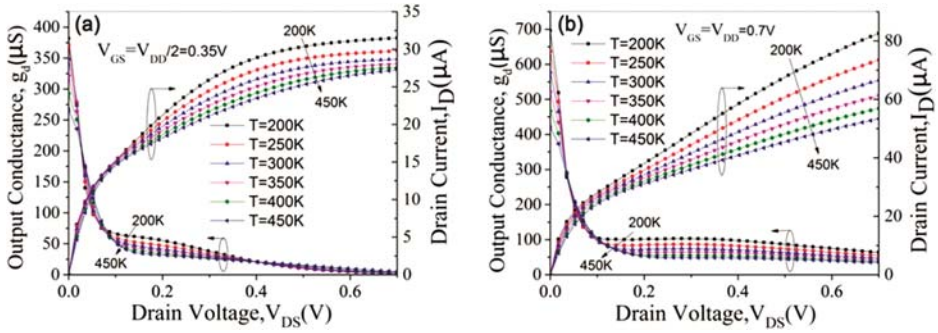

Fig. 4 – I_D and g_d versus V_{DS} characteristics of ADKUS SOI FinFET with temperature variation at (a) V_{GS}=0.35 V and (b) V_{GS}=0.7 V.

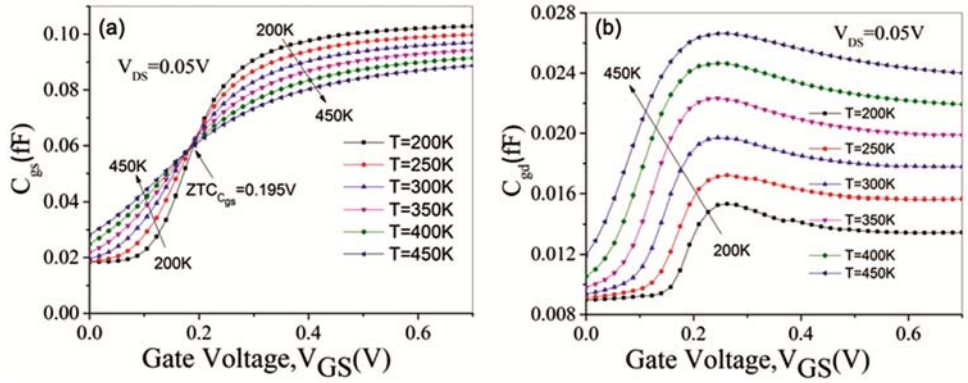

Fig. 5 – Capacitance characteristics of ADKUS SOI FinFET with temperature variation at V_{DS}=0.05 V (a) C_{gs} - V_{GS} and (b) C_{gd} - V_{GS}.

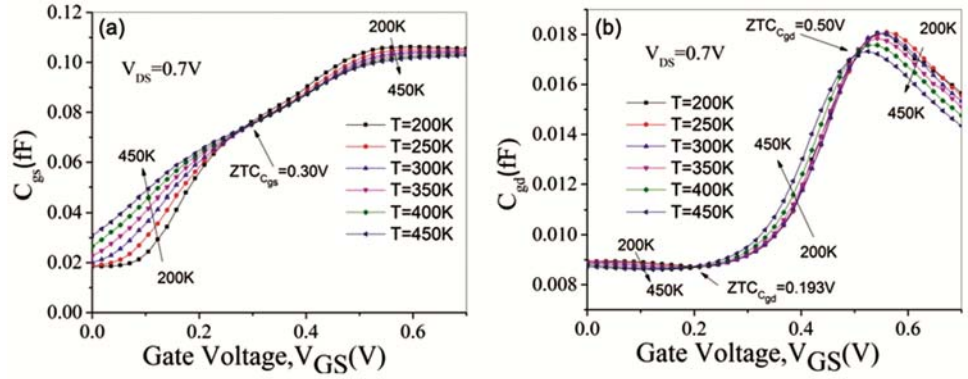

Fig. 6 – Capacitance characteristics of ADKUS SOI FinFET with temperature variation at V_{DS}=0.7 V (a) C_{gs} - V_{GS} and (b) C_{gd} - V_{GS}.

field modulation of high-k and low-k spacers at the drain side. So the optimum value of C_{gd} can be generated for wide temperature range according to required DC and analog/RF circuit applications.

The cut-off frequency $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$ is an important parameter for evaluating the RF performance of ADKUS FinFET. The cut-off frequency (f_T) versus V_{GS} characteristics with temperature variation at V_{DS}=0.05 V and V_{DS}=0.7 V are shown in Fig. 7 (a) and (b), respectively. It is noticed from the Fig.7 that in weak inversion region improvement in cut off frequency (f_T) occurs on increasing the temperature while opposite nature of cut off frequency (f_T) occurs in strong inversion region. At V_{DS}=0.7 V, above the ZTC point of f_T, improvement in f_T occurs due to the steep improvement of charge carrier mobility for a low value of temperature range.

Table 2 shows the some extracted performance parameters for ADKUS SOI FinFET at V_{DS}=0.7 V for a wide temperatures range. From the extracted results of Table 2, it is noticed that there is improvement in intrinsic delay (CV/I), energy-delay product (EDP), off state power dissipation (PD = I_{off}*V_{DD}), SS value, $g_{m,max}$(S), I_{on}/I_{off} and Q-Factor ($g_{m,max}$/SS) for low value of temperature. Q-factor and EDP are important figures of merit for circuit applications and these parameters improved due to the low value of SS and intrinsic delay at low temperature.

Analog/RF performance parameters like g_m, g_d, A_v(g_m/g_d), V_{EA}, C_{gg}, C_{gs}, C_{gd} and f_T for ADKUS SOI FinFET for wide temperature range (200 K-450 K) are also evaluated at V_{DS}=0.7 V and shown in Table 3. It is noticed from Table 3 that there is a significant improvement in intrinsic gain (A_v) and much improvement in cut-off frequency (f_T) at a lower value of temperature. This improvement occurs due to the increased value of g_m at lower temperature range.

4 Implications for Practice

Today world economy directly or indirectly depends on the semiconductor industries. In early days, consumer products like mobile phone, car, watch and even refrigerator have more power as compare to the early computers. Now, we are moving fast towards and more connected world, a world of internet of things where our consumer appliances are able to communicate each other with the more efficient with less cost. This is being possible only due to improvement in the basic unit (transistor) of chip industries. More numbers of transistors integrated into the chip increase the more

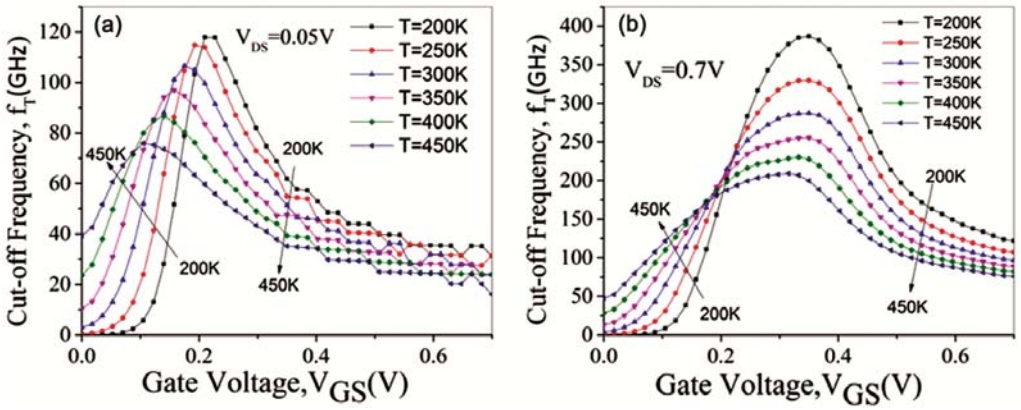

Fig. 7 – Cut-off frequency (f_T) versus V_{GS} characteristics with temperature variation at (a) V_{DS}=0.05 V and (b) V_{DS}=0.7 V.

Table 2 – Extracted performance metrics of ADKUS SOI FinFET for various temperatures at V_{DS}=0.7 V.

Temperature(K)	Energy (CV^2) (Joule) $\times10^{-17}$	Delay (CV/I) (ps)	EDP (Js) $\times10^{-28}$	PD (I_{off}*V_{DD}) (nW)	SS (mV/decade)	I_{on}/I_{off}	V_{th}	$g_{m,max}$ (S) $\times10^{-4}$	Q-factor ($g_{m,max}$/SS) $\times10^{-3}$
200	4.546	2.412	1.097	0.066	44.186	8.62×10^5	0.233	2.29	5.18
250	4.487	2.470	1.108	1.335	54.758	3.77×10^4	0.215	1.93	3.53
300	4.458	2.511	1.119	10.33	65.303	4.42×10^3	0.199	1.67	2.56
350	4.452	2.537	1.129	45.29	76.022	9.26×10^2	0.179	1.47	1.94
400	4.468	2.556	1.142	136.6	89.967	2.86×10^2	0.159	1.30	1.45
450	4.502	2.576	1.160	316.3	107.47	1.16×10^2	0.135	1.16	1.08

Table 3 – Extracted analog/RF performance parameters for ADKUS SOI FinFET for various temperature values at V_{DS}=0.7 V.

Analog/RF extracted performance metrics	Temperature= 200 K	Temperature= 250 K	Temperature= 300 K	Temperature= 350 K	Temperature= 400 K	Temperature= 450 K
g_m(μS)	225	190	164	146	130	115
g_d(μS)	3.53	3.11	2.61	2.63	3.64	5.39
A_V(dB)	36.10	35.69	35.97	34.88	31.09	26.59
V_{EA}(V)	8.92	9.57	11.00	10.67	7.59	5.05
C_{gg}(aF)	92.8	91.6	91	90.9	91.2	91.9
C_{gs}(aF)	82.8	81.6	81	80.8	80.9	81.2
C_{gd}(aF)	9.94	9.94	9.96	10.1	10.3	10.7
C_{gs}/C_{gd}	8.33	8.22	8.13	8.02	7.83	7.58
f_T(GHz)	387	330	287	255	228	200

functionality of consumer products like mobile phones, tablets, computer peripherals, industrial automation equipment, military and security applications. More transistors on a single chip can be done with smaller size transistor with less power consumption and this can be done by FinFET transistor technology. Chips can perform more and more tasks while becoming smaller at the same time, thus enabling their use in countless devices that improve our lives in multi-ways. So, with this newly innovated technology, more advance featured electronics gadgets and industrial automated equipment can be implemented at lower cost in the industries which indirectly reflect the economy of a country.

5 Conclusions

In this paper, ADKUS SOI FinFET is explored in terms of performance parameters like intrinsic delay (CV/I), energy-delay product (EDP), off state power dissipation (PD = I_{off}*V_{DD}), SS value, $g_{m,max}(S)$, I_{on}/I_{off} , Q-Factor ($g_{m,max}$/SS) and analog/RF parameters like g_m, g_d, $A_v(g_m/g_d)$, V_{EA}, $C_{gg,}$ C_{gs}, C_{gd} and f_T for wide temperature range (200 K-450 K).The analysis is done on the basis of zero temperature coefficient (ZTC) for drain current and transconductance bias point for low and high-temperature range. Above and below the ZTC point ADKUS SOI FinFET has opposite nature. So, it is concluded that with the help of ZTC point, ADKUS SOI FinFET can be biased for DC, analog and RF applications for wide temperature range and effect of temperature variation on the device performance can be minimized at ZTC bias point. So, effective use of FinFET transistor for particular application improves the performance of semiconductor industry which reflects the economy and business of the country.

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