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Effect of frequency and bias voltage on the electrical and dielectric properties of atomic layer deposited Al/Al_2O_3/ *p*-Si MOS structure at room temperature

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In the present work , the effect of frequency and bias voltage on electrical and dielectric properties of Al/Al_2O_3/*p*-Si structure in which Al_2O_3 dielectric layer is deposited by ALD using TMA and water as precursors, has been studied. The parameters were extracted from C-V and G-V characteristics by varying frequency from 50kHz to 1MHz at room temperature. Experimental results show that dielectric constant (ε'), dielectric loss (ε'') and dielectric loss tangent (tan δ) decrease with increasing frequency, while *ac* conductivity (σ_{ac}) increases with increasing frequency. It is also observed that interface states density, series resistance and thickness of dielectric layer are major parameters which influence electrical and dielectric properties of MOS structure. The present results indicate that ALD films have low interface states density values and show superior properties than samples prepared by other techniques and are promising for future applications.

Keywords: MOS, Al_2O_3, Dielectric properties, Electrical properties

1 Introduction

Metal-oxide-semiconductor (MOS) type structures play a crucial role in many devices especially in microelectronics and optoelectronics applications. In recent years, there has been a growing interest in metal oxides as dielectric materials for stable capacitors in integrated electronic circuits. Study of MOS structure provides an insight into semiconductor surface conditions during device operation. Numerous studies have been conducted and various models were developed for understanding the behaviour of oxide-semiconductor interface and the current transport mechanisms in MOS capacitors[1-3]. It is essential to design and manufacture the better-quality, long-lived and faster Schottky and MOS structures like capacitors, diodes, transistors and integrated circuits. The performance and reliability of these devices are strongly dependent on the formation of insulator layer (native or deposited), interface states (Nss) localized at the semiconductor-insulator interface and the series resistance (Rs). The electrical and dielectric properties of these devices strongly depend on applied voltage and frequency. Hence, an understanding of the effect of frequency and bias voltage on the electrical and dielectric properties is very much crucial for designing MOS devices.

In general, there are several possible sources of error that have to be taken into account which cause deviations of the electrical and dielectric properties of MOS capacitors from ideal behaviour. These include the effects of insulator layer, interface state density (Nss), series resistance and formation of barrier height. At high-frequencies (such that the carrier life time τ is much larger than 1/ω), the charges at the interface states cannot follow an *ac* signal, whereas at low-frequencies they can easily follow the signal. Therefore, the dependence of electrical and dielectric properties on frequency is very crucial while considering the accuracy and reliability of such devices[4-8].

Atomic layer deposition (ALD) has emerged as the technique of choice for the deposition of ultra thin conformal films for gate oxide as well as many other microelectronic applications. Accurate and simple thickness control is possible with ALD due to its self limiting surface reactions. ALD deposited films are typically very flat and the surface quality is extremely good[9-11]. In addition, the ALD technique allows film deposition at modest or low temperatures as compared to chemical vapour deposition (CVD) technique.

Al_2O_3 has much more favourable optical, electrical and dielectric properties. Al_2O_3 is considered as an excellent dielectric because of its large band gap (9 eV) as compared to other metal oxides and large band offsets with silicon. It also serves as a good diffusion barrier. Though Al_2O_3 has relatively low dielectric constant (~9) value as compared to other high-k materials, this is more than twice that of the

widely used SiO_2 which has a dielectric constant of 3.9. Further , aluminium oxide is considered as a technologically attractive material because of its superior thermal and chemical stability on silicon.

In the present work, thin films of Al_2O_3 were prepared by atomic layer deposition and the effect of bias voltage and frequency on the electrical and dielectric properties of Al/Al_2O_3/ p-Si structure has been studied.

2 Experimental Details

MOS structures ($Al/Al_2O_3/Si$) were fabricated on *p*-type (100) silicon wafer having resistivity of 1-100 ohm-cm. For fabrication process, the Si wafer was cleaned by the standard RCA method[12]. Cleaned wafers were immediately transferred to the ALD chamber. Trimethyl aluminium (TMA) and water were used as precursors and high purity nitrogen as carrier gas. In the ALD chamber, the film growth took place in a 'cyclic manner' at a pressure of 0.480 mbar. One cycle consisted of four consecutive steps: (1) exposure to the precursor which contain metal, (2) nitrogen purge, (3) exposure to H_2O and (4) nitrogen purge. With process optimized, each growth cycle took 33 s. It was observed that thickness of the Al_2O_3 layer increases at a linear rate of 1.2 Å/cycle at a deposition temperature of 225°C. Details of the deposition system and the growth models are given elsewhere[13,14].

Thickness of Al_2O_3 layer was estimated from the measurement of the oxide capacitance at the strong accumulation region of MOS structure[1]. This thickness and refractive index of the deposited layers were also cross verified with spectroscopic ellipsometer (J. A Woollan Co. M 2000U) measurements. In the present study, samples of thickness 58 Å were used. Circular dots of 400 µm diameter and 1000 Å thick aluminium contacts were deposited on the dielectric surface through a metal shadow mask by thermal evaporation at a vacuum of 10^{-5} mbar. Back contacts of high purity aluminium layers were also deposited by thermal evaporation on the backside of the wafer after etching the back side oxide by buffered HF dip. Fabricated structures were annealed at 400°C in forming gas (H_2/N_2) for one hour. The capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) measurements were carried out in the frequency range 50 kHz-1 MHz, respectively using a Fluke PM6306 programmable RCL meter with varying test signal of 50 mVrms. All measurements were carried out with the help of a computer through an IEEE 488 interface and ADC card at room temperature.

3 Results and Discussion

3.1 Electrical properties

The electrical and dielectric properties of MOS structures have been studied from *C-V* and *G-V* characteristics by varying frequency from 50 kHz- 1 MHz. RCL meter was controlled by a data acquisition software program. The conductance technique[1,3] is based on the conductance losses resulting from the exchange of majority carriers at the interface and majority carrier band of the semiconductor when a small *ac* signal is applied to the metal-oxide-semiconductor (MOS) structures. The applied *ac* signal causes the Fermi level to oscillate about the mean position governed by the *dc* bias.

Figure 1 shows the *C-V* and *G*/ω-*V* characteristics for $Al/Al_2O_3/Si$ structure at different frequencies. The overall behaviour is indeed that of an MOS device with distinct regions of accumulation, depletion and inversion. The values of capacitance and conductance

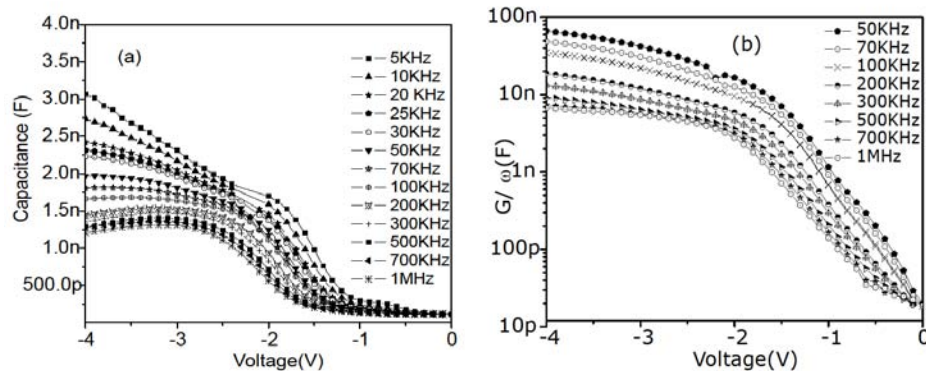

Fig. 1 — Frequency dependence of (a) *C-V* and (b) (*G*/ω)-*V* characteristics of Al/Al_2O_3/ *p*-Si MOS structure at room temperature

depend on the bias voltage and frequency (Fig. 1). The measured values of C and G/ω at accumulation and depletion region decrease with increasing frequency. This is an indication of the presence of interface states (Nss) localized at semiconductor/oxide interface. The capacitance of such an inhomogeneous layer at the semiconductor/oxide interface acts in series with the oxide capacitance causing frequency dispersion[1]. This is due to the fact that at lower frequencies, the interface states can follow the *ac* signal and yield an excess frequency dependent capacitance. In high frequency region since the interface states cannot follow the *ac* signal, the contribution of interface state capacitance to the total capacitance is negligibly small[1,15]. Thus, increase in capacitance towards low-frequency in the accumulation region can be considered to be due to interfacial space charge formation[15,16].

At a given frequency, most of the errors in the C–V and G/ω–V characteristics are due to series resistance (Rs) occurring in the strong accumulation region and a portion of the depletion region. The error can be minimized by measuring the Rs and applying a correction to the measured C and G/ω values before the desired information is extracted[1]. When the MOS structure is biased into strong accumulation, the frequency-dependent properties of MOS devices can be described via the complex impedance. Series resistance is the real part of complex impedance[1,15] as:

$$R_s = \frac{G_{ma}}{G_{ma}^{\ 2} + (\omega C_{ma})^2} \qquad \ldots(1)$$

where C_{ma} and G_{ma} are the measured capacitance and conductance, respectively. The capacitance of the interfacial oxide layer (C_{ox}) is obtained as:

$$C_{0x} = C_{ma}\left[1 + \left(G_{ma}/\omega C_{ma}\right)^2\right] \qquad \ldots(2)$$

Figure 2 shows the variation of Rs as a function of bias voltage in the frequency range 50 kHz-1 MHz and Rs has a peak value. Peak position shifts towards negative bias voltage from −0.4 V to −0.9 V as the frequency increases from 50 kHz to 1 MHz. It can also be observed that as the frequency increases peak value decreases and almost disappears at high frequencies (>500 kHz). Such behaviour of Rs is attributed to the particular distribution of localized Nss at Si/Al_2O_3 interface states and the insulator layer

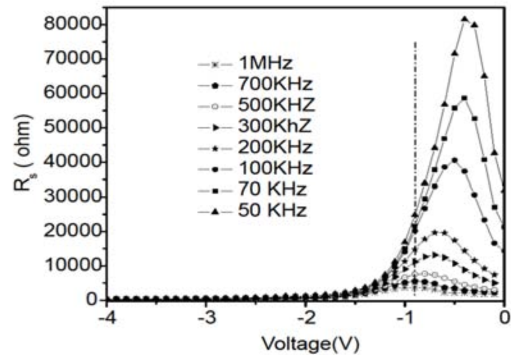

Fig. 2—Variation of Rs of $Al/Al_2O_3/p$ –Si structure as a function of the bias voltage at varied frequencies

at the Al/p-Si interface. This type of behaviour is reported in the case of $Al/TiO_2/p$-Si structure[15,30] also.

3.2 Dielectric properties

Dielectric contact (ε'), dielectric loss (ε''), loss tangent ($\tan\delta$), *ac* electrical conductivity (σ_{ac}) and electric modulus were calculated from the knowledge of capacitance and conductance of $Al/Al_2O_3/p$-Si (MOS) structure in the frequency range 50 kHz-1 MHz at room temperature.

The complex permittivity[17,18] can be written as:

$$\varepsilon^* = \varepsilon' - i\varepsilon'' \qquad \ldots(3)$$

where ε' and ε'' are the real and the imaginary part of complex permittivity, respectively and i is the root of −1. The complex permittivity formalism has been employed to describe the electrical and dielectric properties of Al_2O_3. The relation ship between ε^* and admittance Y^* is given as:

$$\varepsilon^* = \frac{Y^*}{j\omega C_0} = \frac{C}{C_0} - i\frac{G}{\omega C_0} \qquad \ldots(4)$$

where C and G are the measured capacitance and conductance of the dielectric material, respectively and ω the angular frequency ($\omega = 2\pi f$) of the applied electric field[20]. The real part of the complex permittivity-the dielectric constant (ε') at the various frequencies is calculated using the measured capacitance values at the strong accumulation region[19,20] from the relation.

$$\varepsilon' = \frac{c}{C_o} = \frac{c d_{ox}}{\varepsilon_0 A} \qquad \ldots(5)$$

where C_o is capacitance of an empty capacitor, A the electrode contact area, d_{ox} the Al_2O_3 layer thickness and ε_0 is the permittivity of free space (ε_0=8.85*10^{-14} F/cm). In strong accumulation region, the maximum capacitance of the MOS structure corresponds to oxide capacitance (C_{ox}). The imaginary part of the complex permittivity-the dielectric loss (ε''), at various frequencies is calculated using the measured conductance values from the relation,

$$\varepsilon'' = \frac{G}{\omega C_o} = \frac{G d_{ox}}{\varepsilon_0 \omega A} \quad ...(6)$$

The loss tangent (tan δ) can be expressed[17,20] as follows :

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} \quad ...(7)$$

The *ac* electrical conductivity (σ_{ac}) of the dielectric material[17,21,23] is given by the following equation :

$$\sigma_{ac} = \omega C \left(d_{ox} / A \right) \tan\delta = \varepsilon'' \omega \varepsilon_0 \quad ...(8)$$

The complex impedance (Z*) and complex electric modulus (M^*) formalisms were discussed by various authors with regard to the analysis of dielectric materials[20,24]. Analysis of the complex permittivity (ε*) data within the Z^* formalism (Z^* = 1/Y* = 1/iωCoε*) is commonly used to separate the bulk and the surface phenomena and to determine the bulk *dc* conductivity of the material[22,23]. The complex permittivity (ε*) data were transformed into the M^* formalism using the following relation:

$$M^* = \frac{1}{\varepsilon^*} = M' + iM'' = \frac{\varepsilon'}{\varepsilon'^2 + \varepsilon''^2} + i\frac{\varepsilon''}{\varepsilon'^2 + \varepsilon''^2} \quad ...(9)$$

The frequency dependence of the ε′, ε″ and tan δ of $Al/Al_2O_3/p$-Si structure at different voltages is shown in Fig. 3 (a, b and c), respectively. The values of the ε′, ε″ and tanδ calculated from the measured capacitance and conductance values were found to be strong functions of applied voltage, especially at low frequencies. Also, it is evident from Fig. 3 that the values of ε', ε '' and tan δ are almost independent of voltage at high frequencies. In principle at low frequencies, all the four types of polarization processes i.e., the electronic, ionic, dipolar, and interfacial or surface polarization contribute to the values[3,24,25] of ε' and tan δ.

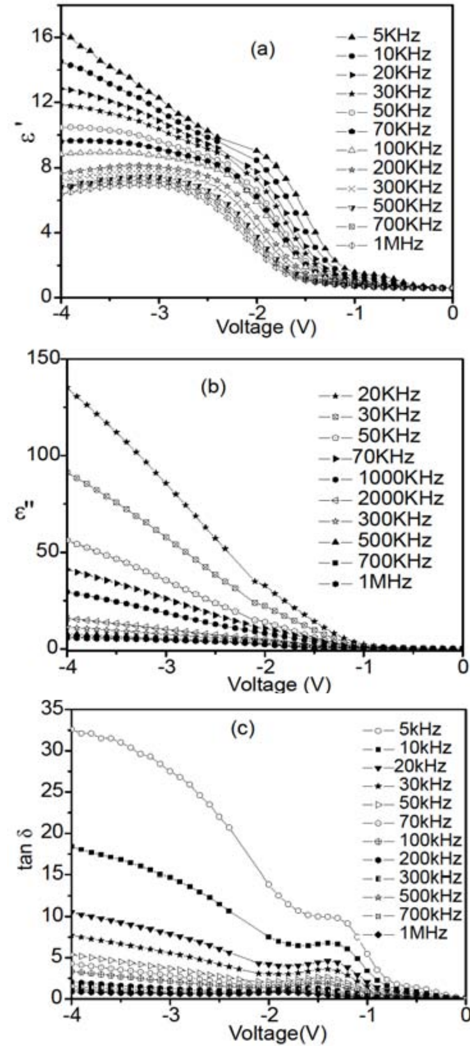

Fig. 3—Frequency dependence of (a) dielectric constant, (b) dielectric loss and (c) loss tangent of $Al/Al_2O_3/p$-Si structure at room temperature

At accumulation region, the values of ε′, and ε″ were found to be as 9.85 and 58.03, 8.19 and 13.08, 5.85 and 3.81 at 50 kHz, 100 kHz and 1 MHz, respectively. On increasing the frequency, the contributions of the interfacial, dipolar or the ionic polarization become ineffective leaving behind only the electronic part. The values of ε′, ε″ and tan δ decrease as the frequency is increased. It is explained by the fact that as the frequency is raised, the interfacial dipoles have less time to orient themselves

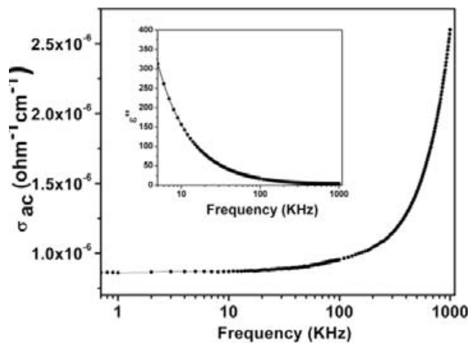

Fig. 4—Frequency dependence of *ac* conductivity of Al/Al_2O_3/p-Si structure at room temperature. The inset shows dielectric loss as a function of frequency

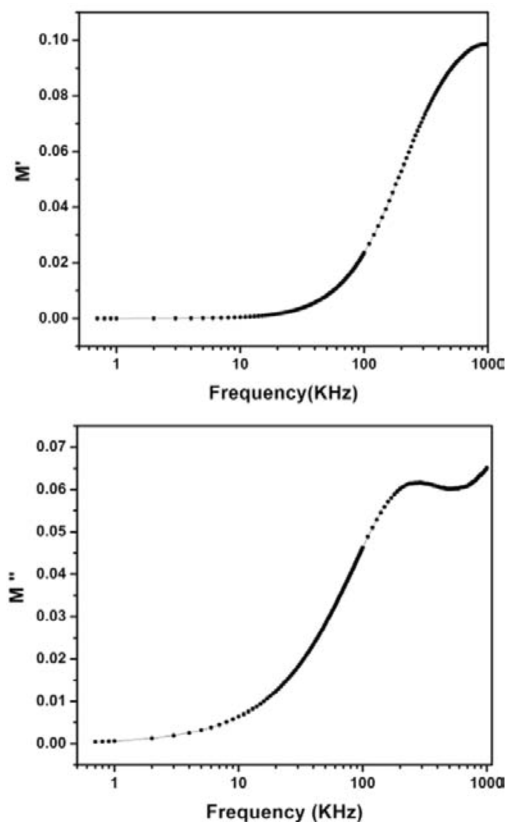

Fig. 5—Real part *M*' and imaginary part *M*'' of electronic modulus *M** versus frequency of $Al/Al_2O_3/p$-Si structure at room temperature

in the direction of the alternating field[26-29]. Especially, in the high frequency range, the value of ε′ becomes closer to ε″. The carrier lifetime of interface trapped charges (τ) are much larger than 1/ω at very high frequency (ω). Similar behaviour was observed by several dielectric materials[1,15].

Figure 4 shows the dependence of *ac* electrical conductivity (σ_{ac}) on frequency. σ_{ac} is independent of frequency upto about 100 kHz and thereafter, increases sharply. σ_{ac} depends on dielectric loss as observed in Fig. 4 and its inset. Dielectric loss decreases with increasing frequency and accordingly the value of σ_{ac} increases. This result is found to be in agreement with the literature[15], where it is suggested that the increase in *ac* conductivity with increasing frequency is attributed to the series resistance effect[30].

Figure 5(a) and (b) show the frequency dependent changes in the real (*M*′) and imaginary (*M*″) components of the electric modulus of the Al/Al_2O_3/p-Si (MOS) structure at room temperature. The *M*' and *M*″ components of the electric modulus increase with increasing frequency. The values of both are close to zero at low frequencies. It is clear that at high frequencies the period (*T*) is very much lower than the lifetime (τ) of interface states. Therefore, the interface states (*N*ss) cannot follow an *ac* signal at these frequencies and the electrical modulus reaches the maximum value corresponding to $M_\infty = 1/\varepsilon_\infty$ due to the relaxation. Similar studies have been reported in literature[15, 24, 25].

4 Conclusions

The voltage and frequency dependence of dielectric properties of $Al/Al_2O_3/p$-Si structure prepared by ALD has been studied in the wide range of frequency from 50 kHz to 1 MHz at room temperature. Experimental results verified that the values of ε′, ε″ and tan δ decrease with increasing frequency. The *ac* conductivity and the electric modulus values increase with increasing frequency for each bias voltage. The observed high values of ε′ and ε″ at low frequencies are attributed to conductivity which are directly related to the increase in the mobility of localized charge carriers at interface states. Also charges in the interface states can easily follow the *ac* signal at low frequencies and yield an excess capacitance. This depends on the relaxation time of the interface states and the frequency of *ac* signal. Series resistance of the structure decreases with increasing frequency. It is concluded that the electrical and dielectric properties of $Al/Al_2O_3/p$-Si structure depend on frequency, dielectric layer thickness, the density of interface states and series resistance. The same parameters cause the deviation from the ideal behaviour of the dielectric characteristics of atomic layer deposited Al_2O_3.

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