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I – V characterization of vacuum deposited zinc selenide – silicon hetero junction

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Zinc selenide (ZnSe) thin films were grown on silicon (Si) wafer by thermal evaporation and the hetero-structure was subjected to annealing at various temperatures. X-ray diffractogram recorded for various samples were analysed to extract the structural information including crystallite size, strain and dislocation density. ZnSe films exhibited cubic structure with (111) orientation and the crystallite size has increased from about 21 nm to 43 nm upon annealing at 673 K. Annealing at temperature above this has degraded the films. I – V characterization has shown nonlinear relation and affected by post deposition annealing. Thermionic emission and Cheung models were applied to obtain various parameters that assess the performance of hetero-structured devices. Minimum ideality factor was observed (n = 1.75 from Cheung Model) for as deposited system and it increased after annealing. Analysis has proven that series resistance increases after annealing under air ambience.

Keywords: Chalcogenides; thin films; hetero-structure; Thermionic emission; Cheung model

1 Introduction

ZnSe, an important member from II-VI group compound semiconductors, finds application in various optoelectronic devices[1-3]. Direct bandgap of 2.7 eV at 300 K makes it an ideal candidate for visible-light optoelectronic devices including blue laser diode[4]. There are several reports on II-VI/IV superlattices which are suitable for numerous applications including photo-detectors, laser diodes and photovoltaics[5-9]. ZnSe/Si is the less studied combination, and this may be due to lattice mismatch of about 4.4%. Thin films deposited on Si wafer have their electrical and optical properties governed by factors like mismatch in lattice constants, thermal expansion and defect states. Controlled combination of strain, composition and thickness can tailor the device properties which can be achieved through deposition parameters and post deposition treatments. Even though electrical conduction mechanism in hetero-structure is influenced by several factors, it is mainly dominated by carrier traps which could be either located at discrete energy levels or distributed exponentially within the band gap[6]. Thermionic emission (TE) and space charge limited conduction are commonly observed mechanisms that control the electrical conduction in hetero-structures and they are dominating at different bias voltages[10].Post growth treatment like annealing has profound influence on crystallite size, strain and dislocation density of the materials which in turn can control the electrical properties[3, 11-13]. Hence the present report is focussed on electrical properties of vacuum deposited ZnSe/Si hetero-structure and the effect of post deposition annealing on these properties. Analysis of I-V characteristics is carried out with TE and Cheung Model.

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2 Experimental Methods

ZnSe thin films of about 100 nm have been grown on Si wafer with <100> orientation by thermal evaporation technique at a residual pressure of about 10^{-6} mbar. High purity (99.999%) ZnSe compound has been deposited at 0.2 nm/s rate on 350 μm thick wafer. Evaporation rate and thickness of the films have been monitored by digital thickness monitor operated at 6MHz. Pristine (S1) and samples annealed at different temperatures 473 K (S2), 573 K (S3), 673 K (S4), 773 K (S5) have been characterized for structural and electrical properties. X-ray diffractogram has been recorded with Rigaku Miniflex – 600 diffractometer operating at 40 kV with Cu - Kα (Average wavelength 0.1542 nm). I – V characterization has been carried out using computer interfaced Keithley 2450 source meter setup at room temperature under dark condition with aluminium as contact electrode on either side.

Table 1 — Structural parameters of hetero-structure obtained from XRD

Samples	Material	2θ (deg)	d (±8%) (nm)	hkl	a =b =c (nm)	Cell Volume ($\times10^{-3}$nm^3)	D (nm)	Strain (10^{-4})	Dislocation density ($\times10^{14}$m^{-2})
S1	Si	68.35	0.144	100	0.144	2.98	65.8	2.50	3.96
	ZnSe	26.23	0.358	111	0.620	238.53	21.6	18.86	21.12
S2	Si	69.40	0.142	100	0.142	2.86	61.1	2.66	4.60
	ZnSe	27.45	0.342	111	0.593	208.58	23.0	16.94	18.63
S3	Si	69.38	0.142	100	0.142	2.86	61.4	2.65	4.55
	ZnSe	27.57	0.341	111	0.591	205.92	29.0	13.38	11.72
S4	Si	69.38	0.142	100	0.142	2.86	64.6	2.51	4.11
	ZnSe	27.50	0.342	111	0.592	207.47	43.2	9.00	5.28
S5	Si	69.35	0.142	100	0.142	2.86	65.2	2.49	4.04
	ZnSe	No prominent peak has been observed							

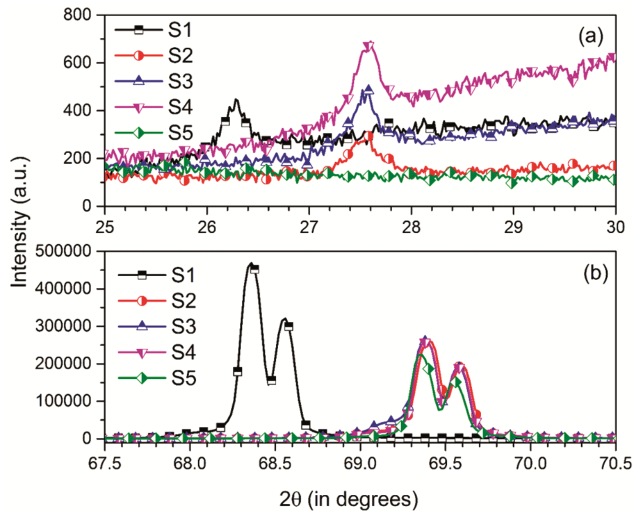

Fig. 1 — X-ray diffractogram showing peaks corresponding to (a) ZnSe and (b) Si for pristine and annealed samples of ZnSe/Si hetero - structures

3 Results and Discussion

Structural characterization

X-ray diffractogram recorded for ZnSe/Si hetero-structure is depicted in Fig. 1 (ab). Double peaks observed for silicon can be attributed to Kα1 and Kα2 from the X-ray source. Qualitative analysis of the XRD pattern shows significant shift in the peak position for both ZnSe and Si. Various structural parameters have been extracted from XRD pattern and listed in Table 1. Scherrer formula provides the crystallite size (D) from the FWHM of XRD peak.

$$D = \frac{0.94\lambda}{\beta cos\theta} \quad \text{... (1)}$$

where β is FWHM for the peak observed at θ and λ is the wavelength of X-ray source. For cubic structure of the crystal, (h k l) is related to lattice constant a as follows.

$$\frac{1}{d^2} = \frac{h^2 + k^2 + l^2}{a^2} \quad \text{... (2)}$$

whered is interplanar spacing. The strain (ε) induced in the crystal can be evaluated using following relation.

$$\varepsilon = \left[\frac{\lambda}{D\cos\theta} - \beta\right] \times \frac{1}{\tan\theta} \quad \text{... (3)}$$

Finally, the dislocation density (δ) can be estimated with the following Eq. [14]:

$$\delta = \frac{15\varepsilon}{aD} \quad \text{... (4)}$$

Compare to as-deposited ZnSe films, crystallite size has increased upon annealing. Dislocations are incorporated into the crystal system due to several reasons like thermal stress, mechanical stress, vacancies *etc*. Dislocations are different from point defects since they are not thermodynamically stable defects and their presence increases the free energy of the crystal. In the present investigation, the strain induced and dislocation density in the films have shown downward trend with increase in temperature. It is the established fact that dislocation density, total dislocation length per unit volume, can be reduced by prolonged annealing. Regardless of deposition techniques, development of stress in the films is unavoidable. Shift in the peak position of the pattern indicates that the strain is mostly uniform in the film and it may be mainly originated due to lattice mismatch between Si wafer and ZnSe films. Annealing has resulted in reduction of the residual stress in the films which may be due to reduction in the defects as observed from XRD analysis. It may also be due to densification which is evident from the decrease in the cell volume. However, annealing at relatively higher temperature has affected the film crystallinity negatively and the XRD peak has

disappeared (S5). Annealing has shown marginal effect on Si wafer also. After annealing, peak height has reduced considerably as compared with the pristine samples. Apart from that, no much change has been observed in dislocation density and cell volume for Si wafer.

I – V characterization

I – V data recorded for different ZnSe/Si hetero-structure samples are shown in Fig. 2. The I – V characteristic of hetero – structures are strongly influenced by properties of the interface. From the I – V plot, it is evident that current is nonlinearly related to voltage and it has exhibited good rectification. Furthermore, the samples undergone annealing treatment has shown variation in I – V characteristics as compared with the pristine samples.

In-depth study of the I – V characteristic of these samples has been carried out with thermionic emission and Cheung models. From thermionic emission model, current follows the voltage in accordance with the following Eq.[14]:

$$I = I_s exp\left(\frac{qV}{nkT} - 1\right) \quad \text{... (5)}$$

where k is the Boltzmann constant, n the ideality factor, q the electronic charge and T is the temperature. Also, I_s, the reverse saturation current, is given by [15]:

$$I_s = AA^{**}T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \quad \text{... (6)}$$

Where A is effective area of the device of the device, A^{**} is Richardson constant and ϕ_B is barrier height. For the applied bias voltage $V > 3kT/q$, the above equation can be approximated as,

$$I = I_s exp\left(\frac{qV}{nkT}\right) \quad \text{... (7)}$$

Hence, from the plot of ln (I) Vs. V (Fig. 3) ideality factor and reverse saturation current can be extracted. Parameters extracted for different samples using TE model is listed in Table 2. It is interesting to note that ideality factor has increased for all annealed samples except S5.

Even though thermionic emission model provides the important diode parameters like ideality factor and barrier height, it ignores the effect of series resistance. To overcome this drawback, Cheung had proposed modification to the diode equation in which the effect of diode series resistance Rs is modelled as a series combination of a diode and resistor[16];

$$I = I_S \, exp\left(\frac{q(V - IR_S)}{nkT}\right) \quad \text{... (8)}$$

Differentiation of the above equation yields,

$$\frac{dV}{d(ln\, I)} = R_s I + \frac{nkT}{q} \quad \text{... (9)}$$

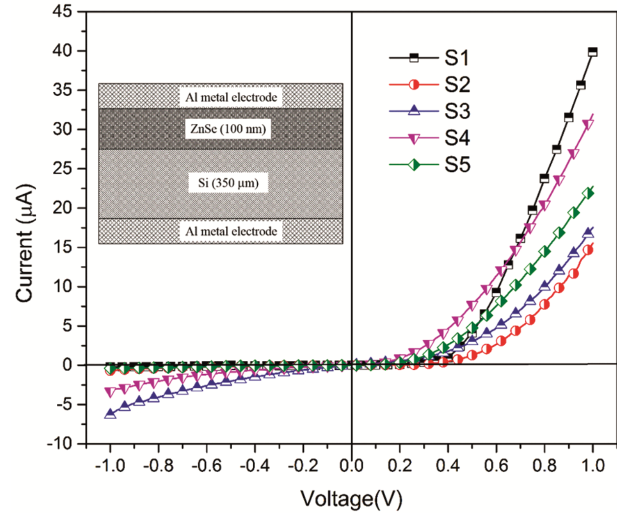

Fig. 2 — I - V characteristics of pristine and annealed ZnSe/Si hetero-structures (Inset: device structure)

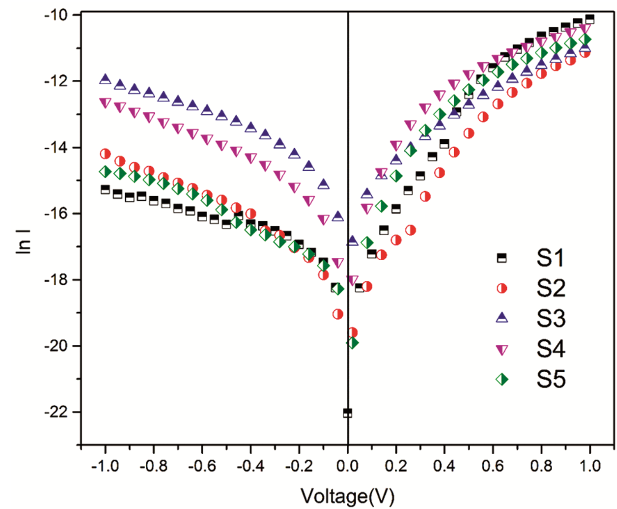

Fig. 3 — Plot of ln(I) *vs.* V for pristine and annealed ZnSe/Si hetero-structures

Table 2 — Parameters extracted with TE Model and Cheung Model

Samples	TE Model			Cheung Model		
	I_s(nA)	n	Φ_B(eV)	n	Φ_B(eV)	R_s(kΩ)
S1	14	3.526	0.848	1.756	0.957	11.2
S2	64	3.597	0.879	2.445	0.770	70.9
S3	144	5.897	0.795	2.141	0.878	78.0
S4	126	4.096	0.802	1.979	0.812	92.9
S5	336	3.318	0.836	2.236	0.855	38.2

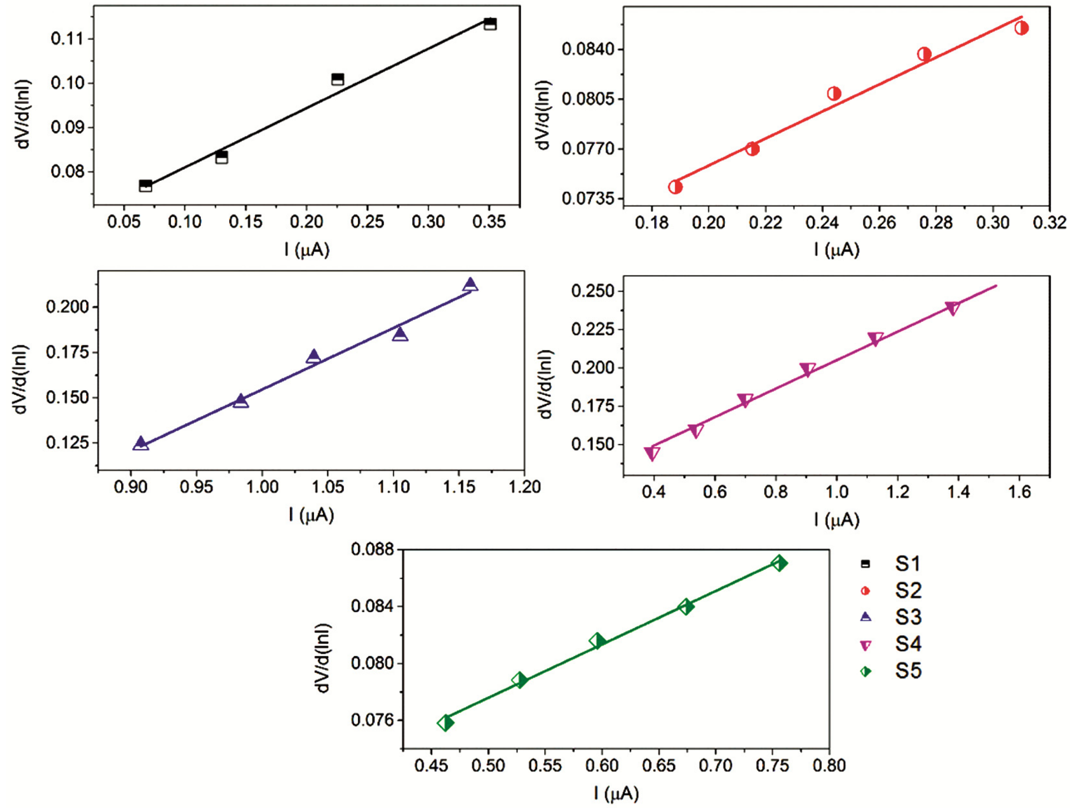

Fig. 4 — Plot of dV/d(ln (I)) *vs.* I for pristine and annealed ZnSe/Si hetero-structures

Figure 4 depicts the plot of dV/d(ln I) for different samples from which series resistance Rs and ideality factor n are extracted. To obtain barrier height ϕ_B, new function $H(I)$ is defined[15] such that,

$$H(I) = R_S I + n\phi_B \quad \text{... (10)}$$

where,

$$H(I) = V - \frac{nkT}{q} ln\left(\frac{I}{AA^{**}T^2}\right) \quad \text{... (11)}$$

H(I) vs. I for different samples is depicted in Figure 5. Table 2 compares the various junction parameters obtained from TE and Cheung model. It is interesting to note that Cheung model yielded lower ideality factor for all the samples, as compared with TE model. Moreover, difference between ideality factors obtained in the two models has shown strong correlation with series resistance having correlation coefficient equal to 0.87. This suggests that the influence of series resistance cannot be neglected while extracting the junction parameters for hetero-structures.

Even though the device performance is decided by several factors, in hetero-structures, it is significantly affected by high density of misfit dislocations at the interface[17]. This is inevitable in the continuous films formed over a crystalline substrate or multi-layer thin film devices. Even though defect free interface is far from attainment, the choice of deposition or growth conditions and post deposition heat treatment can alter the interface properties considerably[18]. In the present investigation, series resistance has been minimum for as-deposited hetero-structure (Sample S1) and it has increased with increase in annealing temperature (Samples S2, S3, S4). Lattice mismatch and defects in the films lead to strain in the films which has profound influence on electrical properties of semiconductors[19]. Strain in the films mainly affects the grain size[11] where increase in the strain results in reduces gain size. However, in the present study, strain has reduced upon annealing. Still the series resistance has shown upward trend which leads to conclude that, apart from strain; some other parameter is also affecting the series resistance. Since the annealing has been performed under atmospheric pressure, incorporation of oxygen and formation of oxide states could be the reason of observed increase in the series resistance. Similar behaviour is reported for diodes with silicon substrates[20].

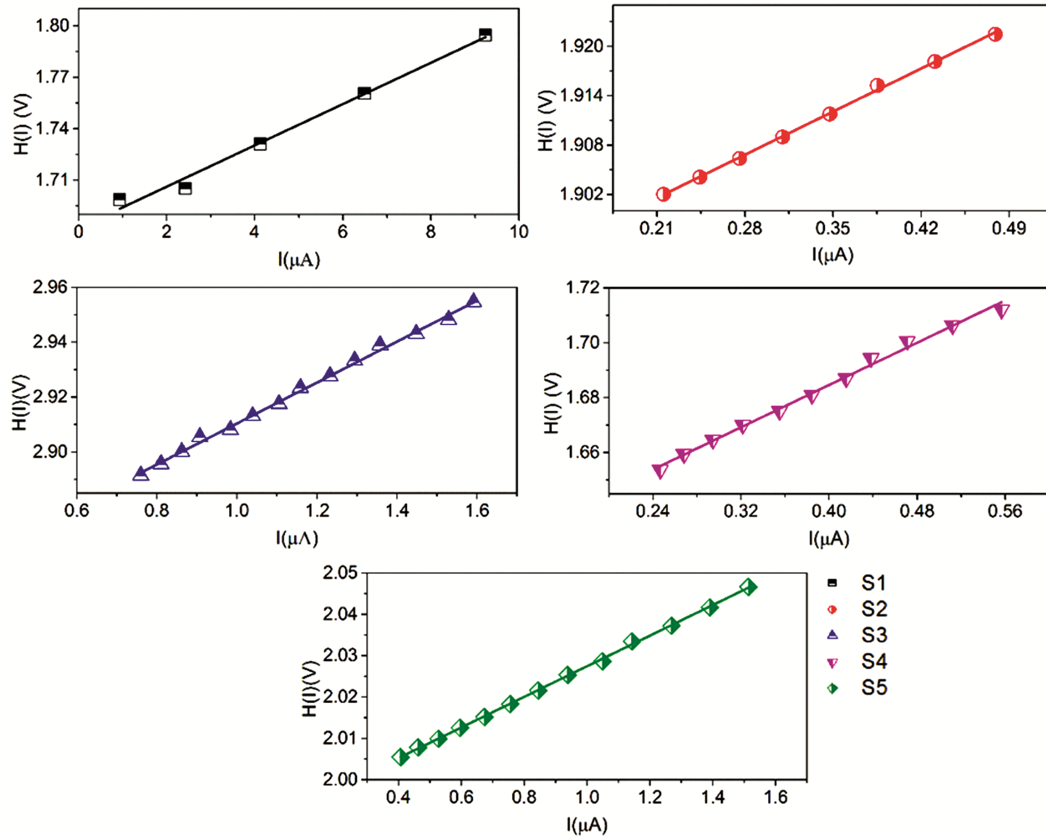

Fig. 5 — Plot of H(I) Vs. I for pristine and annealed ZnSe/Si hetero-structures

4 Conclusion

Vacuum deposited ZnSe/Si hetero-junction has shown non-linear I – V relation. Detailed analysis has revealed that annealing temperature strongly influences hetero-structure parameters. Lattice constant for as-deposited ZnSe films is higher than the bulk value and the difference has reduced due to annealing. So, it can be concluded that annealing the films help in reducing the strain apart from increase in crystallite size. Even though strain in the films has reduced upon annealing, series resistance has increased which could be due to incorporation of oxygen and formation of oxide states. The difference in the ideality factor calculated with and without considering the series resistance has shown strong correlation with R_s having coefficient of correlation about 0.87. Hence, it could be decided that series resistance of the hetero-structure has to be considered for the junctions with higher values of R_s.

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