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# Design of SOI MOSFETs for Analog/RF Circuits

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In this paper, the concept of integration of a high voltage trench MOSFET (HVT MOSFET) and low voltage trench MOSFET (LVT MOSFET) is proposed. Insulator (Dielectric) isolation technique is used for the implementation of HVT and LVT MOSFETs on Silicon-on-Insulator (SOI) layer side by side. The HVT MOSFET consists of two gates which are placed in separate trenches in the drift region. The proposed structure minimizes ON-resistance ($R_{on}$) along with increased breakdown voltage ($V_{br}$) due to reduced electric field, creation of dual channels, and folding of drift region in vertical direction. In HVT MOSFET, the drain current ($I_D$) increases leading to enhanced trans conductance ($g_m$) by simultaneous conduction of channels which improves the cut-off frequency ($f_t$) and maximum oscillation frequency ($f_{max}$). On the other side, LVT MOSFET consists of a gate placed within a $SiO_2$ trench to create two channels on either side of gate. The parallel conduction of two channels provides enhancement in $I_D$, $g_m$, $f_{max}$ and $f_t$. The performance analysis of HVT MOSFET and LVT MOSFET is carried out using 2D simulation in the device simulator (ATLAS).

**Keywords**: Trench-gate, MOSFET, Breakdown voltage, Trans conductance, High-frequency

## Introduction

Power integrated circuits (PICs) are gaining importance due to increasing demand[1, 2] of systems which consumes less energy, and fulfilled the manufacturing and economic constraints with efficient, rugged and reliable features for applications such as an a log integrated power amplifiers (IPAs), industrial control circuits, automobile electronics, personal communication peripherals, programmable logic circuits, convenient power systems etc[3, 4]. In PICs, integration of different electronic devices is carried out to achieve the entire circuit on same chip to get a better product in terms of power consumption, reliability, size, weight, and cost[4–6]. In such systems, metal-oxide-semiconductor field-effect transistors (MOSFETs) are often used as key components for small signal (low voltage) as well as large signal (high voltage) analog/RF amplification. Therefore, it is important to study the integration of low voltage and high voltage MOSFETs on same chip. For analog/RF circuits, the important performance parameters of a power MOSFET are output drive current ($I_D$), breakdown voltage ($V_{br}$), specific on-resistance ($R_{on,sp}$), trans conductance ($g_m$), maximum oscillation frequency ($f_{max}$) peripherals and cut-off frequency ($f_t$). On the other hand, for a low voltage MOSFET, $I_D$, $g_m$, $f_{max}$ and $f_t$ are considered for evaluating the analog/RF performance.

In the recent past, trench-gate power laterally-diffused MOSFET (LDMOSFET) structures on Silicon-on-Insulator (SOI) as a mature material have been reported to achieve substantial improvement in all performance parameters[7–9]. These trench-gate LDMOSFETs are designed to have multi-gates which create more than one channel in parallel and hence provide higher $I_D$ and lower $R_{on,sp}$. In these devices, the trench based architecture causes improved reduced-surface field (RESURF) effect which helps to provide the full depletion of the drift layer so a significant enhancement in$V_{br}$[10–12]. Moreover, the simultaneous control of multi-gates over drive current provides higher $g_m$ leading to substantial gain in frequency response of the LDMOSFET. Further, there are some reports[13–15] in which the suitability of trench-gate based MOSFETs on SOI have been demonstrated for small signal analog/RF circuits with superior performance in terms of $I_D$, $g_m$, $f_t$ and $f_{max}$[16,17]. The high performance trench based LDMOSFETs and low voltage MOSFETs can be utilized in PICs on SOI to obtain highly reliable, energy efficient, light weight,

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small size and cost effective solution to many analog/RF applications[18,19]. Therefore, main focus of this work is to propose the integration of high voltage trench (HVT) MOSFET and low voltage trench (LVT) MOSFET on SOI for analog/RF circuits. The RF performance of both the devices is evaluated using 2D simulations in the TCAD simulator (ATLAS)[20].

**Device structure and its mechanism**

Figure 1 illustrates the integration of insulator-isolated high voltage trench MOSFET (HVT MOSFET) and low voltage trench MOSFET (LVT MOSFET). Both the devices are realized in *n*-type Si epitaxial layer on SOI. The proposed HVT MOSFET and LVT MOSFET are isolated using a $SiO_2$ trench. Both structures are trench-gate MOSFETs in which *n*-channels are created in *p*-region vertically. The drain electrodes are separated from source/gate regions by thick oxides ($SiO_2$) filled in trenches. The drain current ($I_D$) starts to flows over all the channels instantaneously from drain to source electrodes.

The HVT MOSFET consists of a trench-gate architecture with unequal oxide thickness ($t_{ox}$ = 30 nm, and$t_{ox1}$ = 0.3 µm). In HVT MOSFET, gate length (L) = 0.5 µm and cell pitch length ($L_p$) =3 µm with other lengths i.e. $L_1$ and $L_2$ equal to 1.42 µm and 0.58 µm, respectively. The doping of n-drift region ($N_d$) is $8\times10^{16}$ and p-body doping is $1.5\times10^{16}$ $cm^{-3}$. The trench depth ($t_1$) and epitaxial thickness ($t_e$) are kept 1.25 µm and2.2 µm, respectively. A positive gate bias ($V_{GS}$) forms dual channels in p-region along the side-walls of gate trenches leading to flow of $I_D$ in parallel. The conduction of both channels in parallel enhances the $I_D$ and reduces the $R_{on,sp}$. The mechanism which controls of $I_D$ simultaneous by both the gates improves the $g_m$ which leads to better $f_t$ and $f_{max}$ of the HVT MOSFET.

On other side of the structure, LVT MOSFET is implemented with 1920 nm thick *n*-type Si layer with doping consideration of $10^{19}$ $cm^{-3}$ over SOI substrate. The *p*-region thickness is taken 40 nm with doping consideration of $2\times10^{18}$ $cm^{-3}$. The thickness of $n^+$-cap layer is 20 nm with doping consideration of $1\times10^{19}$ $cm^{-3}$. This $n^+$-cap layer is used to take Ohmic source contacts. The gate is placed at the centre of structure in a $SiO_2$ trench. TaN is used as a gate material with work function of 4.5 eV and gate oxide thickness of 2 nm. The application of $V_{GS}$ higher than threshold voltage forms two channels in p-region parallel to the side-walls of the gate so that the conduction of $I_D$ occurs in parallel leading to higher $I_D$ and $g_m$ of the LVT MOSFET. The improvement in $g_m$ results in higher $f_t$ and $f_{max}$ of the LVT MOSFET.

**Physical Models and Fabrication Process**

The HVT and LVT MOSFET structures are implemented in the simulator (ATLAS) and various models are in voked to simulate the characteristics of devices. For simulation of HVT MOSFET, concentration dependent mobility (CONMOB) model

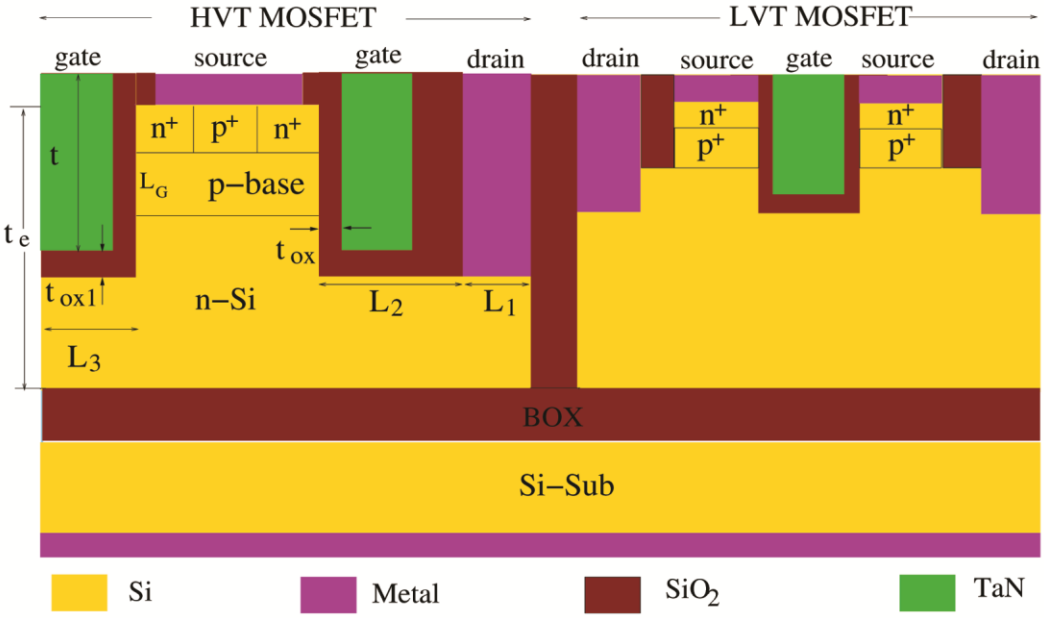


Fig. 1 — 2D structure of insulator-isolated HVT MOSFET and LVT MOSFET.

and electric field dependent mobility (FLDMOB) are taken to determine the mobility of carriers. *Shockley-Read-Hall* (SRH) model is used for the charge carrier formation related phenomenon. AUGER model is employed for high-level injection effects due to high current density features. For simulation of LVT MOSFET, in addition to SRH model, Lombardi (CVT) model is taken to incorporate the effect of mobility and scattering mechanism due to lattice vibrations. The band gap narrowing (BGN) model is included to account the effects of doping level on valence band and conduction band. In this study, we consider trap-charge density of $1\times10^{12}$ $eV^{-1}$ $cm^{-2}$ at the interface of $Si/SiO_2$ is also incorporated.

Fabrication steps of the insulator-isolated HVT MOSFET and LVT MOSFET are shown in Fig. 2. All fabrication steps are created with the help of ATHENA process simulator. Initially, consider *n*-Si layer with thickness 2 µm on SOI with doping $1.5\times10^{16}$ $cm^{-3}$. In both the MOSFETs, $p^+$, *p*-base, and


Fig. 2 — Fabrication and design step of the insulator-isolated HVT MOSFET and LVT MOSFET.

$n^+$ regions are formed with the ion implantation method. The HVT MOSFET and LVT MOSFET are separated by each other by an oxide layer as shown in Fig. 2(i). In next step, by taking different masks, trenches are formed as depicted in Fig. 2(ii). In subsequent step, deposition of $SiO_2$ occurs over the entire wafer as shown in Fig. 2(iii). Figure 2(iv) illustrates the etching of $SiO_2$ to obtain the value $t_{ox}$=30 nm for HVT MOSFET and $t_{ox}$= 2 nm for LVT MOSFET. After this, deposition of $n^+$ poly-silicon takes place over the entire wafer as shown in Fig. 2(v). In next step, etching of $n^+$ poly-silicon occurs as shown in Fig. 2(vi). The proposed structure is obtained by etching of Si from the surface as shown in Fig. 2(vii). At last, for creation of gate, source, and drain contacts, metallization and patterning is done as illustrated in Fig. 2(viii).

## Results and Discussion

2-D simulations of proposed structure, insulator-isolated HVT MOSFET and LVT MOSFET, are carried out by considering the ATLAS (device simulator)[20]. The accuracy of simulation models is determined by comparing the simulated results with pre-fabricated experimental data of a MOSFET[21] as shown in Fig. 3. The measured device consists of 2.5 nm oxide thickness with 150 nm gate-length. The buried oxide and the SOI layers thickness are 400 and 45 nm, respectively. The proposed device consists of 2 nm oxide thickness with 40 nm gate-length. It consists of 1920 nm thick *n*-type Si layer and buried oxide thickness is 400 nm. We observed that there is a good agreement between simulation and experimental outcomes. Using the calibrated models, *V-I* characteristics of HVT MOSFET are obtained at different $V_{GS}$ as depicted in Fig. 4. The electron passing through the channel drift with a constant saturation velocity ($v_s$), the current ($I_D$) = $qnv_sA$. The observed value of $I_D$ is 0.16 mA/μm in HVT MOSFET at $V_{DS}$ (drain to source voltage) =15 V and $V_{GS}$=3 V. At $L_G$ of 40 nm, *V-I* characteristics of LVT MOSFET at different $V_{GS}$ are shown in Fig. 5. At $V_{DS}$ =2 V and $V_{GS}$ =1V, $I_D$ of LVT MOSFET is 2.32 mA/μm due to creation of two channels in p-body. LVT MOSFET consist gate oxide thickness of 2 nm and gate length is 40 nm. On other side of the structure, HVT MOSFET consist oxide thickness of 30 nm and gate length is 0.5 μm. In LVT MOSFET due to small gate oxide thickness as well as small gate

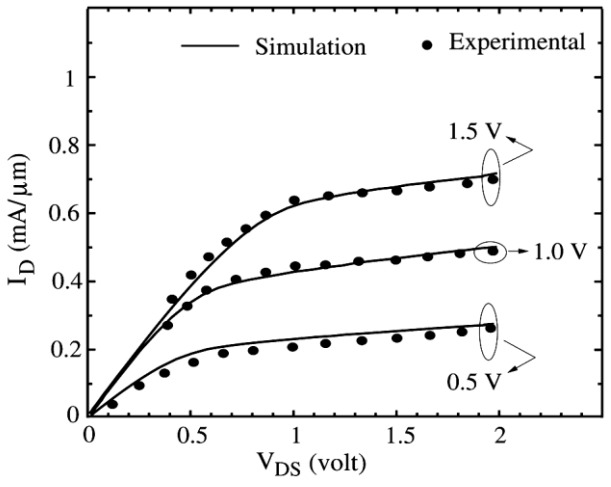


Fig. 3 — Experimental and Simulated I-V Characteristics of a MOSFET [16].

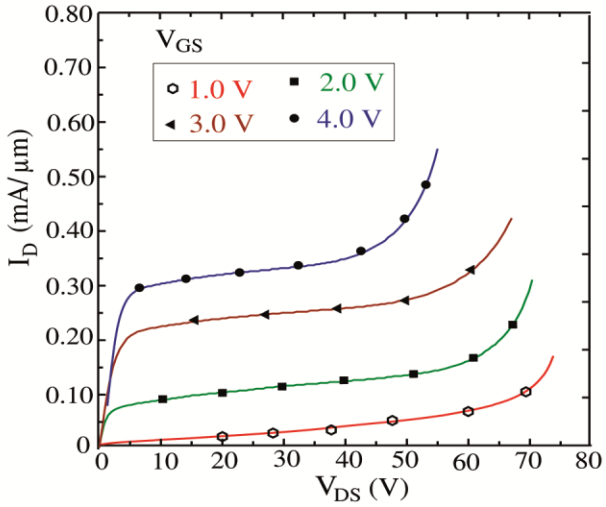


Fig. 4 — I-V Characteristics of HVT MOSFET.

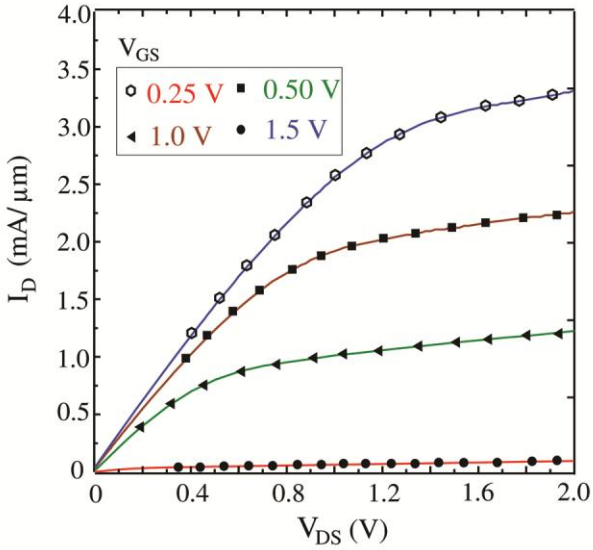


Fig. 5 — I-V Characteristics of LVT MOSFET.

length, the device performs higher $I_D$ and $g_m$ in comparison to HVT MOSFET[3].

Figure 6 gives the variation of $g_m$ of the HVT MOSFET with $V_{GS}$ axes. The device exhibits high $g_m$ which basically represents the gain of MOSFET. The value of $g_m$ is calculated as $\Delta I_D/\Delta V_{GS}$. The peak value of $g_m$ for the proposed HVT MOSFET is 0.140 mS/μm at $V_{GS}$ of 2.75 $V$ due to instantaneous control of drive current by two gates. On the other side, for LVTMOSFET, maximum obtained value of $g_m$ is2.102 mS/μm at $V_{GS}$=1.5 V as depicted in Fig. 7. The device structure with high $g_m$ demonstrates its suitability for RF amplifier applications[22].

The $f_t$ is the unity current gain cut-off frequency. The value of $f_t$ is calculating at 0 dB gain. The value of $f_t$ is measured where maximum gain occurs[16]. The $f_{max}$ is the maximum oscillation frequency, for calculating its value $R_g$ and $C_{gd}$ values are taken into consideration. The microwave frequency characteristics ($f_{max}$ and $f_t$) of MOSFETs are calculated using the following equations [17][22-23]:

$$f_t = \frac{g_m}{2\pi C_t} \quad \ldots (1)$$

where total capacitance, $C_t = (C_{gd} + C_{gs})$, $C_{gd}$ signifies the gate to drain capacitance and $C_{gs}$ signifies the gate to source capacitance of the MOSFET.

$$f_{max} = \left(\frac{f_t}{2\pi R_g C_{gd}}\right)^{1/2} \quad \ldots (2)$$

where $R_g$ represents the gate electrode resistance of the MOSFET. The value of $R_g$ is 370 Ω.

Another important parameter is the $g_m/I_D$ ratio concerned in an analog circuits designing. It represents the efficiency for conversion of dc power into ac gain. This ratio is helpful to find out the inversion level in a LVT MOSFET. Lower the value of $g_m/I_D$ shows a strong inversion whereas; a higher value specifies a weak inversion in the channel. From Figure 8, $g_m/I_D$ ratio decreases as the $I_D$ increases and the operating point transfers towards strong inversion. It shows the good short channel effects immunity in the proposed MOSFET[16, 24].

The $f_{max}$ and $f_t$ of HVT MOSFET are shown in Fig. 9. The $f_t$ for HVT MOSFET is evaluated at a value of $V_{gs}$ = 1.7 V, where maximum gain occurs[16]. For proposed HVT MOSFET, the value of $f_t$ obtained is 6.25 GHz, while $f_{max}$ is found to be 17 GHz. For LVT MOSFET, the frequency characteristics are shown in Fig. 10. For LVT MOSFET $f_t$ is evaluated at a value of $V_{gs}$ = 2.75 V. For LVT MOSFET, the value

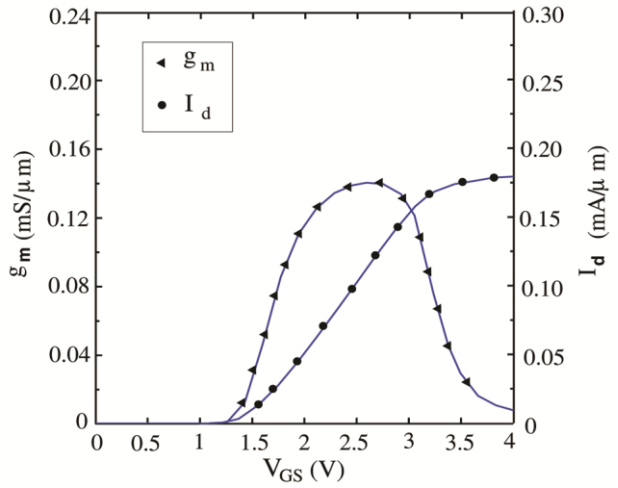


Fig. 6 — $g_m$-$I_d$ Characteristics of HVT MOSFET.

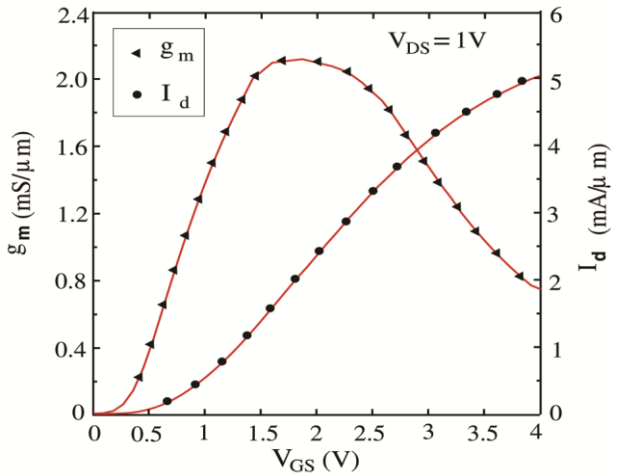


Fig. 7 — $g_m$-$I_d$ Characteristics of LVT MOSFET.

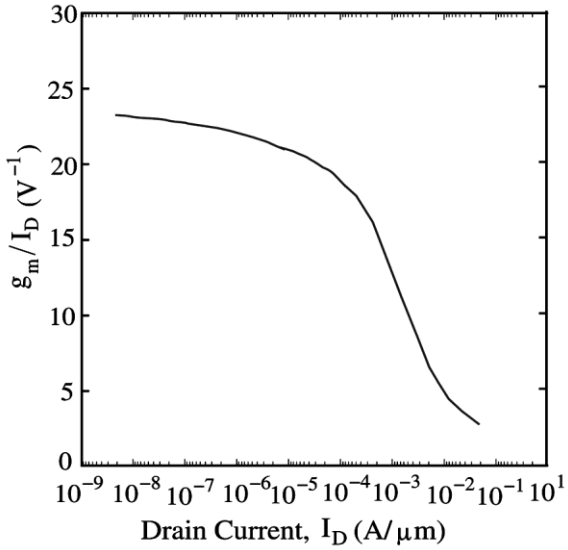


Fig. 8 — $g_m/I_D$ Characteristics of LVT MOSFET.

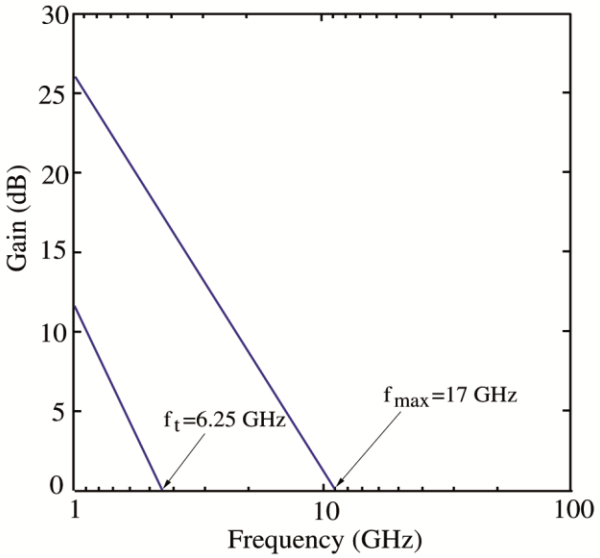


Fig. 9 — Frequency characteristics of the HVT MOSFET.

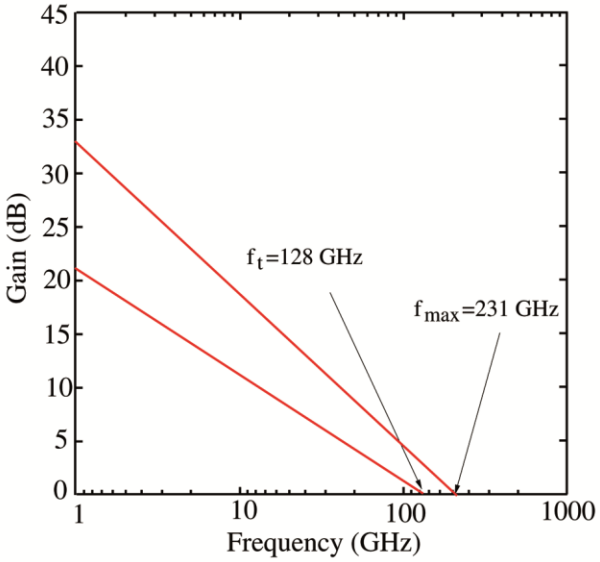


Fig. 10 — Frequency characteristics of the LVT MOSFET.

of $f_t$ and $f_{max}$ is found to be 128 GHz and 231 GHz, respectively. The value of $R_g$ is 370 Ω.

Figure 11 shows the variation of gate-drain capacitance ($C_{gd}$) and the gate-source capacitance ($C_{gs}$) for the HVT MOSFET. The $C_{gd}$ is found to be 0.91 fF/μm and $C_{gs}$ is 2.65 fF/μm. Figure 12 shows the variation of $C_{gd}$ and $C_{gs}$ for the LVT MOSFET. The $C_{gd}$ is found to be 1 fF/μm and $C_{gs}$ is 1.61 fF/μm. Higher the $g_m$, and lower $C_{gs}$, $C_{gd}$ obtained in the proposed structure so higher the $f_t$. It is very useful for high-frequency applications[19].

Figure 13 shows the sub-threshold (SS) curves of the LVT MOSFET. In the sub-threshold region, the

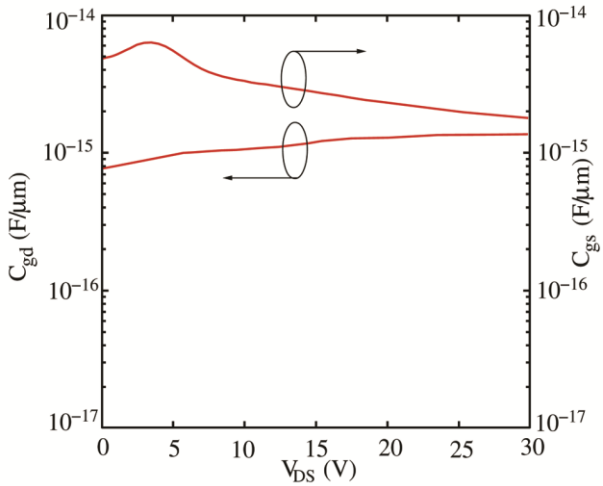


Fig. 11 — $C_{gd}$ and $C_{gs}$ of the HVT MOSFET.

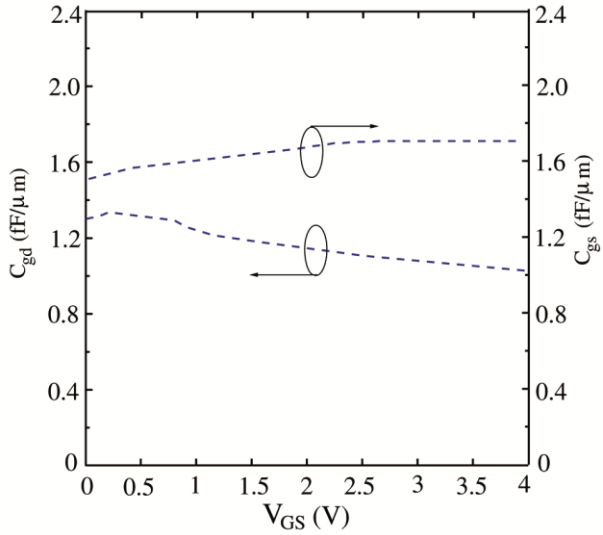


Fig. 12 — $C_{gd}$ and $C_{gs}$ of the LVT MOSFET.

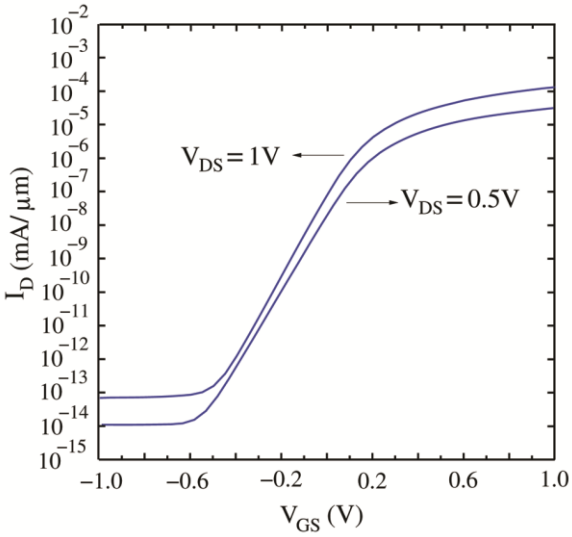


Fig. 13 — Sub-threshold curves of the LVT MOSFET.

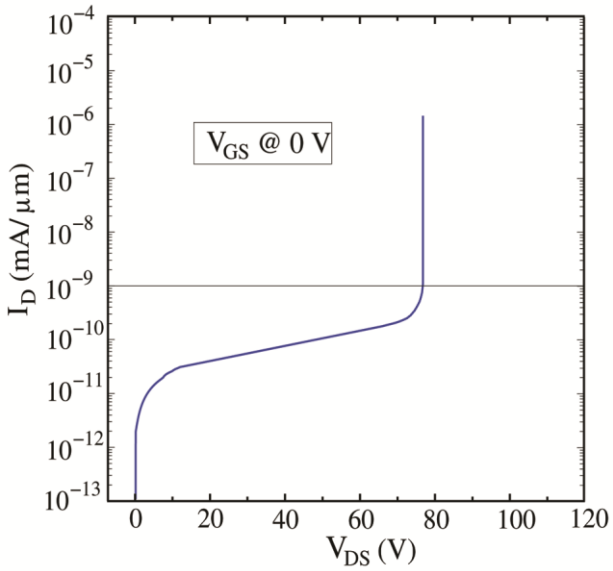


Fig. 14 — Breakdown characteristics of the HVT MOSFET.

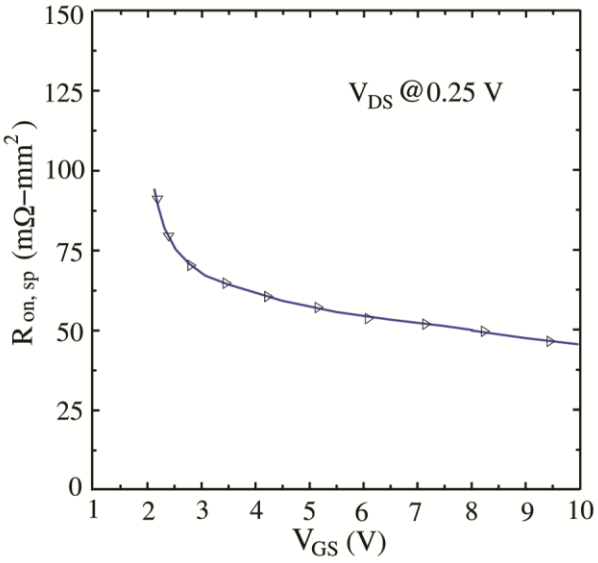


Fig. 15 — Variation of $R_{on,sp}$ along $V_{GS}$ of HVT MOSFET.

Table 1 — A performance parameter comparison of HVT and LVT MOSFETs with other reported MOSFETs

| Device Type | $I_D$ (mA/μm) | $V_{br}$ (V) | $R_{on,sp}$ (mΩ.mm$^2$) | $g_m$ (μS/μm) | $f_t$ (GHz) | $f_{max}$ (GHz) |
|---|---|---|---|---|---|---|
| HVT MOSFET | 0.16 | 78 | 488 | 140 | 6.25 | 17 |
| LVT MOSFET | 2.32 | - | - | 2102 | 128 | 231 |
| C-SOI PICs [13] | - | 39 | 39 | - | - | - |
| SOI PICs [13] | - | 90 | 90 | - | - | - |
| DTG MOSFET [3] | 0.074 | 52 | 51 | 106 | 4 | 10.8 |
| LV MOSFET [3] | 0.53 | - | - | 1033 | 44 | 138 |

$I_D$ is dominated by diffusion and the value of $I_D$= exp [q($V_{GS}$-$V_t$)/kT][22]. The sub-threshold swing is calculated as, SS=$\Delta V_{GS}/\Delta \log I_D$. At $L_G$ of 40 nm and $V_{DS}$ =1 V, the architecture exhibits SS of 84 mV/dec. The drain voltage of a short-channel MOSFET increases from the linear region towards the saturation region, its $V_t$ roll-off becomes larger. This effect is known as DIBL. The drain-induced barrier lowering (DIBL) of the MOSFET is calculated

As DIBL =$\frac{\partial V_t}{\partial V_{DS}}$. The DIBL of the structure is 126 mV/V. The suppressed DIBL of device is caused by small variation in $V_t$ with $V_{DS}$ because the trench gate assists to attain better control of the potential in p-base. At $V_{DS}$ of 1 V, the current ratio (on-to-off) of LVT MOSFET is found to be1.25 x $10^9$. In the literature, for same device and the same channel length, SS=118 mV/dec and DIBL=78 mV/V is observed[3]. It is noted that the proposed MOS consists lower value of SS.

Figure 14 shows the breakdown (Off-state) characteristics of HVT MOSFET. In this study, $V_{br}$ corresponds to the voltage at which $I_D$ value reaches $10^{-9}$ mA/μm[3-4]. The $V_{br}$ of HVT MOSFET is obtained as 78 V. This voltage is achieved by the minimization of electric field in the drift region of proposed structure. The dependence of $R_{on,sp}$ on $V_{GS}$ for the HVT MOSFET is depicted in Fig. 15. The device exhibits low value of $R_{on,sp}$ due to higher draincurrent[4]. Table 1 gives a performance comparison of HVT and LVT MOSFETs with other reported MOSFETs in literature. It is evident from the comparison that the proposed MOSFETs provide significant improvement in terms $I_D$, $g_m$, $f_t$ and $f_{max}$ which make the proposed integration of HVT and LVT structure more suitable for analog/RF circuits.

## Conclusions

In this work, the integration of insulator-isolation of LVT MOSFET and HVT MOSFET for making smart IC on SOI is presented. The architecture of proposed devices is based on trench gates which form multiple conduction channels in the *p*-body to obtained higher output current and lower on-state resistance. The enhancement in $I_D$ results in higher $g_m$ leading to improved frequency characteristics of the

proposed structure. For HVTMOSFET, various parameters are obtained as $I_D$ = 0.16 mA/μm, $R_{on,sp}$ = 45 mΩ.mm$^2$, $g_m$ = 0.140 mS/μm, $V_{br}$ = 78 V, $f_{max}$ = 17 GHz, and $f_t$ = 6.25 GHz. For LVT MOSFET, the performance parameters are; $I_D$= 2.32 mA/μm, $f_{max}$ = 231 GHz, $f_t$ = 128 GHz, $g_m$ = 2102 mS/μm. With the help of 2D analysis in device simulator (ATLAS), the characteristics/performance of LVT MOSFET and HVT MOSFET are evaluated and demonstrated. The result exhibits both devices is having good performance. The proposed integration concept with trench gate technology can be used in power ICs for high-frequency analog circuits.

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