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A Novel Energy Efficient and Process Immune Schmitt Trigger Circuit Design Using FinFET Technology

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Continuous scaling of MOS (Metal oxide semiconductor) devices gives rise to drastic increase in leakage power dissipation, which overall increases the total power dissipation. This happens due to increase in short channel effects. FinFET device has the capability to reduce short channel effects, hence reduces power dissipation as well. In this paper short-gate FinFET (fin type field effect transistor) based Schmitt trigger using LCNT (Leakage Control NMOS transistor) technique is proposed using ASAP7 PDK (A 7nm FinFET Predictive process design kit) at 7nm technology node and comparative analysis is provided with the one without LCNT technique. The simulated results shows that FinFET based Schmitt trigger using LCNT technique reduces average power dissipation and power delay product (PDP) by 36.97% and 35.6%, respectively compared to one without FinFET LCNT technique. The reliability analysis using Monte Carlo approach at ±10% process, voltage and temperature (PVT) variation under 3σ Gaussian distribution shows that LCNT FinFET Schmitt trigger provides better performance compared to FinFET Schmitt trigger at 7nm technology node.

Keywords: ASAP7 PDK; LCNT; FinFET; Schmitt Trigger; PVT

Introduction

At lower technology nodes, leakage power dissipation has become more substantial in Nanoscale CMOS (Complementary Metal Oxide Semiconductor) circuits due to increase in short channel effects. Due to this, evaluation of leakage power is crucial for designing of low power CMOS logic circuits. There exist leakage components in nanoscale CMOS logic circuits. These include reverse bias junction and BTBT (band to band tunneling), gate tunneling and subthreshold leakages. When transistor size is decreased, there is a need to reduce supply voltage as well due to the reason that it can cause electrical breakdown if not reduced. Besides, performance of the device also gets affected. For this threshold voltage is reduced which increases the subthreshold leakage. In order to increase transistor driving strength and to control short channel effects in deep submicron region, gate oxide thickness is also reduced at lower technology nodes. This results in tunneling current through gate oxide which depends on voltage across oxide and gate oxide thickness. In addition to this application of halo doping and higher substrate doping density results in increase in reverse biased junction and BTBT leakage current through source and drain substrate junctions[1,2] To minimize short channel effects and specifically leakage components in CMOS devices, various process level and circuit level techniques are devised from time to time. At circuit level leakage is controlled by controlling the voltage at different terminals of a device, while as in process level reduction of leakage power is obtained by controlling the junction depth, oxide thickness and length of the device. Both types of techniques have certain limitations which can be overcome by the use of new type of devices at lower technology nodes. New type of devices which came into existence has better electrostatic control for carrier flow. These include FinFET, π-gate, Omega-gate and GAA (Gate All Around) devices[3]. Among them, FinFET device is very much similar to the conventional MOSFET (Metal Oxide Semiconductor Field Effect Transistor) in terms of layout and fabrication[4]. Therefore, FinFET acts as a bridge between conventional and modern electronic devices.

One of the important concerns of digital and analog electronic circuits is noise immunity. Hysteresis being the important characteristic of Schmitt trigger becomes cornerstone for noise immunity of Schmitt trigger circuit. It is used to shape input signals in

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electronic circuits and finds its applications mainly in memory design. FinFET based Schmitt trigger has shown better performance as compared to the conventional MOSFET based Schmitt trigger[5,6]. This paper presents the design and analysis of FinFET based Schmitt trigger at 7 nm technology node using ASAP7 PDK[7]. The comparative analysis is provided with the proposed one, *i.e.*, FinFET based Schmitt trigger using LCNT technique. From the comparative analysis it is found that FinFET based Schmitt trigger using LCNT technique offers better performance as compared to the conventional one, i.e., without LCNT technique. The rest of the paper is organized as follows. Section 1 gives the detailed analysis of ASAP7PDK. Section 2 briefly describes the circuit level leakage reducing techniques. Section 3 presents the circuit description of a FinFET based Schmitt trigger at a 7nm technology node using ASAP7PDK. In section 4 LCNT based Schmitt trigger is described and comparative analysis is made with the one without LCNT technique. Section 5 covers the simulation results and discussion. In section 6 reliability analysis is made using the Monte Carlo approach. Finally, the conclusion is presented in section 7.

1 ASAP7 PDK

ASAP7 PDK (A 7 nm FinFET Predictive process design kit) is designed at ASU (Arizona State University) in partnership with ARM research for academic use. This process design kit has a collection of SPICE models (BSIM-CMG) of FinFET device. In addition to this it consists of technology files for cadence virtuoso, DRC (Design Rule checker), LVS (Layout *vs*. Schematic checker) and parasitic extraction *etc*. for 7nm technology node. It consists of four threshold voltages to fulfill the need of both performance and standby power parameters in system on chip designs. All four devices are supported by ASAP7 PDK. These include SLVT, LVT, RVT and SRAM. The highest drive strength is of SLVT and lowest is of SRAM devices in ASAP7 PDK. SRAM devices in ASAP7 PDK can be used for retention latches and other low power circuits due to reduction in GIDL (Gate Induced Drain Leakage) effect which also reduces overlap capacitance. Moreover, ASAP7 PDK consists of fast (FF), typical (TT), and slow (SS) corner models to cover the variety of circuits for power and performance analysis. In our circuit design of Schmitt trigger at 7nm technology, TT corner is used at 7nm technology node[7].

2 Circuit Level Leakage Reduction Techniques

In modern semiconductor industry power dissipation is one of the crucial issues due to increase in leakage power dissipation for lower process technology node [8]. In battery operated portable devices like mobile phones, computers and PDA's (Personal Digital Assistants), power dissipation should be low in order to decrease packaging and cooling costs and also to improve the battery life. Leakage power dissipation contributes major portion of total power dissipation as per ITRS (International technology road map) and it is predicted that it can increase upto 32 times per device. Therefore, need arises to devise leakage reducing techniques.[9,10]

For this various gate level techniques are used to reduce leakage power dissipation. These include transistor stacking, multi-threshold and body biasing etc. In MTCMOS (Multi-threshold CMOS) standby power is decreased by large extent but this technique result in increase in propagation delay due to the presence of high threshold voltage sleep transistors. In addition to this data retention also becomes difficult when sleep transistors are turned off [11]. Body biasing technique also minimizes standby power dissipation by increasing threshold voltage but it requires additional circuitry for body bias[12]. In transistor stacking more than two transistors are turned off to reduce leakage but at the same time area gets increased[13]. Other techniques include LECTOR, GALEOR, ONOFIC, INDEP and LCNT. In LECTOR (LEakage COntrol transisTOR) technique two leakage control transistors (one PMOS and one NMOS) are inserted between pull up and pull-down network. In this technique, the connections are made in such a way that one leakage control transistor is always near cutoff region. This results in decrease in leakage power dissipation. Besides, there is no need of additional circuitry. But this technique increases the propagation delay[14]. Another technique called GALEOR technique has same structure as LECTOR technique but in this case the locations of extra inserted PMOS and NMOS is interchanged. These extra inserted transistors are high threshold voltage transistors causing high resistance to leakage current path[15]. This results in high power saving but it suffers from significant drawback that lower voltage level is

greater than 0V and higher voltage level is less than V_{DD} (supply voltage).

In addition to this ONOFIC technique is also proposed. In this technique ONOFIC block exists between pull up and pull-down network. The leakage reduction in this technique is less as compared to LECTOR but at the same time propagation delay penalty is also reduced [16]. INDEP (input dependent) technique is also one of the leakage reducing techniques. It also uses two extra input dependent transistors between pull up and pull-down network. In this technique inputs to extra inserted input dependent transistors is needed which is to be generated by algorithms. Hence, increases the computational time[17].

There exists another technique which is called LCNT (Leakage control NMOS transistor). This technique has two leakage control NMOS transistors between pull up and pull-down network. As shown in Fig. 1, the gate terminals of both LCNT1 and LCNT2 are connected to output node. Besides, switching of both extra inserted leakage control transistors is also controlled by output node as shown in Fig. 1. When both LCNTs are ON, their series combination results in 2Vt voltage drop, where Vt is the threshold voltage of LCNT transistors. This decrease in voltage drop from supply voltage V_{DD} to ground reduces the power dissipation.

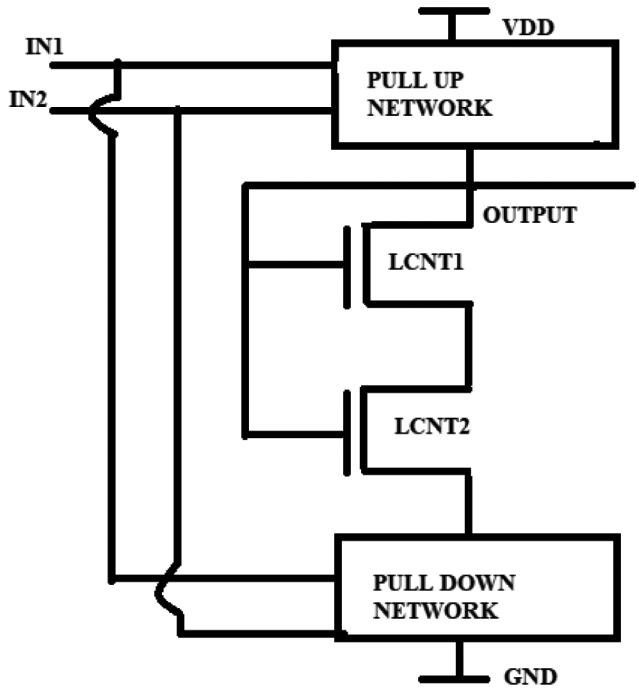

Fig. 1 — Schematic arrangement of LCNT technique.'

LCNT technique uses the single threshold voltage which prevents the performance reduction by multi-threshold voltage circuits. This technique has lesser leakage power dissipation as compared to LECTOR and ONOFIC technique. In addition to this LCNT has lower propagation delay than LECTOR and GALEOR and lesser layout area as compared to other techniques mentioned [18]. The above discussion clearly depicts that LCNT technique can prove as one of the best leakage reduction techniques for FinFET based Schmitt trigger circuit at 7 nm technology node as well. So, in this paper FinFET based Schmitt trigger using LCNT technique is designed at 7nm technology node using ASAP7 PDK and the comparison is provided with the one without LCNT technique. The digital performance parameters are analyzed for both the circuits.

3 FinFET based Schmitt Trigger

Schmitt trigger is a high-performance circuit which converts time varying analog signals to digital pulse signals. It works in a positive feedback mode. Schmitt trigger designed using operational amplifier has some disadvantages like larger area, limited register values etc. This can be overcome by designing of Schmitt trigger using MOS transistors, specifically using CMOS technology implementation. Schmitt trigger is used in modern ADC's (Analog to digital converters) as a comparator circuit and can be used in storage elements like SRAMs as well. It has better noise immunity, hence form the important part of communication circuits. Schmitt trigger is designed using different number of transistors to improve the hysteresis width and supply voltage in order to make noise immunity better[19].

The design of Schmitt trigger using FinFET devices provides improved performance parameters. In this paper Schmitt trigger is designed using FinFET at 7 nm technology node using ASAP7 PDK. It consists of three p-type FinFETs and three n-type FinFETs as shown in Fig. 2. When the input goes from low to high, the n-type FinFETs will be turned ON and the p-type FinFETs will be turned OFF. Due to this p-type FinFET on output side will be turned ON and the output will be constant low signal as shown in Fig. 3. Similarly, when the transition occurs from high to low, p-type FinFETs in the input side will be turned ON and n- type FinFETs will be turned OFF. Hence, turns ON n-type FinFET on output side. As n-type FinFET on the output side is in saturation,

it results in constant high pulse and retains its state unless next transition occurs.

Schmitt trigger circuit provides high noise immunity due to the hysteresis characteristic. The distinct switching thresholds are represented by VTC (voltage transfer characteristics) curves for negative and positive going input slopes [19]. Fig. 4 represents the hysteresis loop created by short gate FinFET Schmitt trigger circuit. The pull-up and pull-down ratio of FinFETs is responsible for switching threshold of the circuit. When the ratio is increased, it increases the switching threshold as well and vice versa. The ratio is adapted according to the direction of transition, hence causes hysteresis effect or shift in threshold. Larger the hysteresis window better is the noise immunity in the Schmitt trigger circuit. The performance of any digital VLSI circuit is measured in terms of following parameters, power dissipation, chip area, stability and speed of operation etc. Continuous scaling in CMOS reduces chip area, power dissipation and production cost. But scaling can be performed upto certain extent due to the fact that at low technology nodes short channel effects increases. Moreover, power dissipation also increases due to increase in sub-threshold leakage at low technology nodes. Hence, reduction of power dissipation is a big challenge in modern- day VLSI circuits, because almost all portable devices run on battery power. In this paper different parameters like average power dissipation, propagation delay and power delay product are calculated for FinFET Schmitt trigger circuit at 7nm technology node as shown in Table 1. In a typical chip made of MOSFETs or FinFET like devices power is dissipated

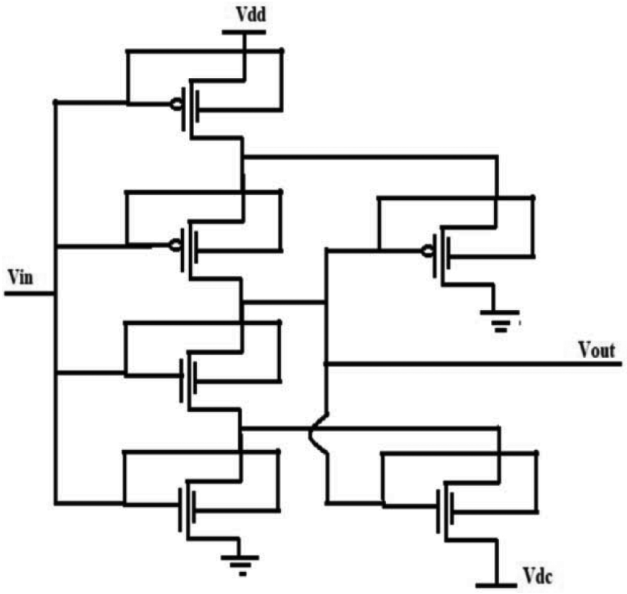

Fig. 2 — Schematic of SG FinFET Schmitt Trigger.

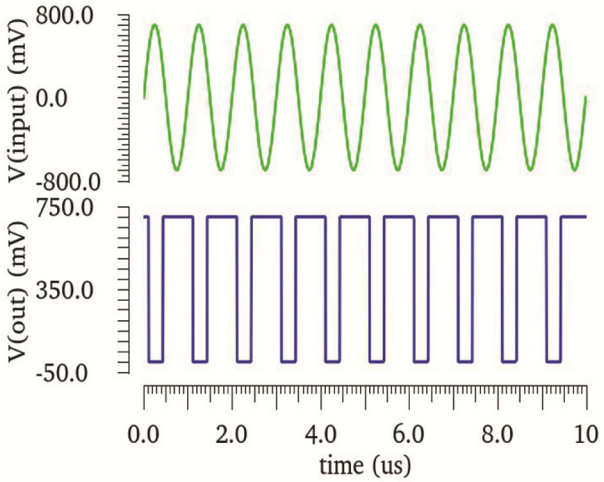

Fig. 3 — Waveform of SG FinFET Schmitt Trigger.

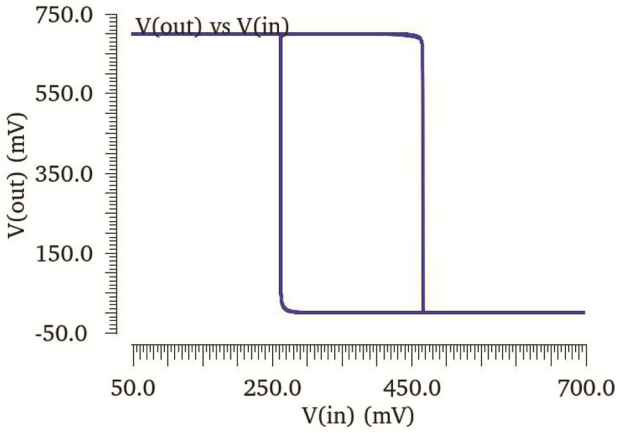

Fig. 4 — DC transfer characteristics of FinFET Schmitt trigger circuit at 7nm technology node.

Table 1 — Comparative analysis of FinFET Schmitt trigger and LCNT FinFET Schmitt trigger.

Performance Metrics	FinFET Schmitt trigger	LCNT FinFET Schmitt trigger	Change (%)	FinFET Schmitt trigger	LCNT FinFET Schmitt trigger	Change (%)
Frequency		1MHz			1GHz	
Power Dissipation (nW)	89.89	56.65	36.97	259.84	165.31	36.38
Propagation Delay(ns)	32.82	33.56	2.10	573.05	839.22	46.44
Power Delay Product(fJ)	2.95	1.90	35.6	148.90	138.73	6.83

whenever current flows from power supply to ground, i.e., Power is drawn from voltage source. In this design average power dissipation is calculated because instantaneous power does not give us a clear picture of how much battery is getting drained because it may happen sometimes that instantaneous power is very high but over long period of time, power consumption is low. So, average power dissipation is more meaningful to calculate than the power drawn at a particular point in time. The other parameter measured for FinFET Schmitt trigger is propagation delay, it is the time required to change output after the application of input. In our design worst case propagation delay is considered. Besides, this power delay product is calculated as shown in Table 1 which is the product of power dissipation and propagation delay of FinFET Schmitt trigger in our case. Lesser the PDP less is the energy consumption in the circuit. Hence, circuits with low PDP are more energy efficient in comparison to the ones with high PDP.

4 FinFET Based Schmitt Trigger with LCNT Technique

FinFET based Schmitt trigger is proposed using LCNT technique. In our case it is used to design FinFET based Schmitt trigger using ASAP7 PDK. It minimizes the leakage power dissipation in FinFET Schmitt trigger circuit. In our design of FinFET Schmitt trigger at 7 nm technology node two n-type leakage control short-gate FinFETs are inserted between pull up and pull-down networks. The switching of these extra inserted n-type FinFETs is controlled by voltage at output node because gate terminals of both leakage control n-type FinFETs are connected to output node as shown in Fig. 5. When input is at logic low level, the n-type FinFETs in pull down network are turned OFF and p-type FinFETs in pull up network are turned ON. Due to this both leakage control extra inserted n-type FinFETs are turned ON. The leakage control n-type FinFETs are in series and this series geometry results in reduction in voltage from output node to ground due to the 2Vt voltage drop. In addition to this two OFF n-type FinFETs in the pull-down region increases the resistance as well. Hence, reduces leakage power dissipation. Now, when the input is at logic high level, both p-type FinFETs in pull up network are turned OFF and n-type FinFETs in the pull-down network are turned ON. Due to this leakage control FinFETs are in cut-OFF region. They provide highest resistance due to stack effect in the path from pull up network to pull down network, which results in leakage current reduction in FinFET Schmitt trigger circuit. Therefore, design of FinFET Schmitt trigger using LCNT technique results in energy efficient design of FinFET Schmitt trigger. The various performance parameters are shown in Table 1 and the waveform obtained is shown in Fig. 6. The hysteresis loop formed by LCNT FinFET Schmitt trigger is shown in Fig. 7.

5 Simulation Results and Discussion

The power dissipation in LCNT FinFET Schmitt trigger is reduced by 36.97% and power delay product is decreased by 35.6% in comparison to the FinFET Schmitt trigger without LCNT technique. However, propagation delay is increased slightly by 2.1% in LCNT FinFET Schmitt trigger at 1MHz frequency. The above analysis clearly depicts that design of FinFET Schmitt trigger with LCNT technique at 7nm technology node using ASAP7 PDK is better in terms of various performance parameters and hence can be used to design FinFET based Schmitt trigger at lower technology nodes without affecting the functionality of FinFET based Schmitt trigger.

The effect of PVT (Process-voltage-temperature) variations on logic circuits is more significant at lower technology nodes. In order to analyse the effect

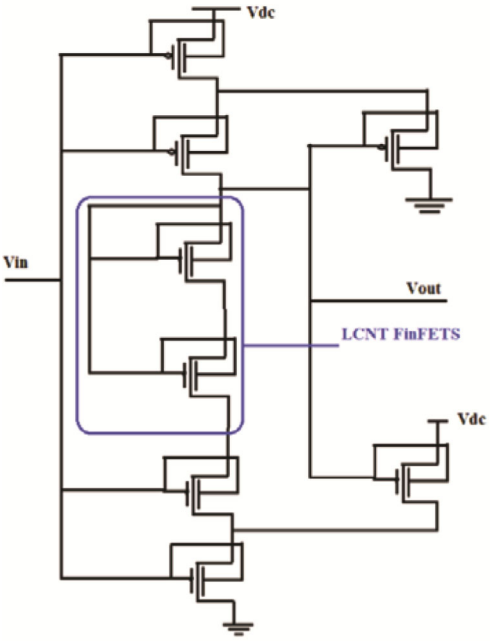

Fig. 5 — Schematic of SG LCNT FinFET Schmitt trigger.

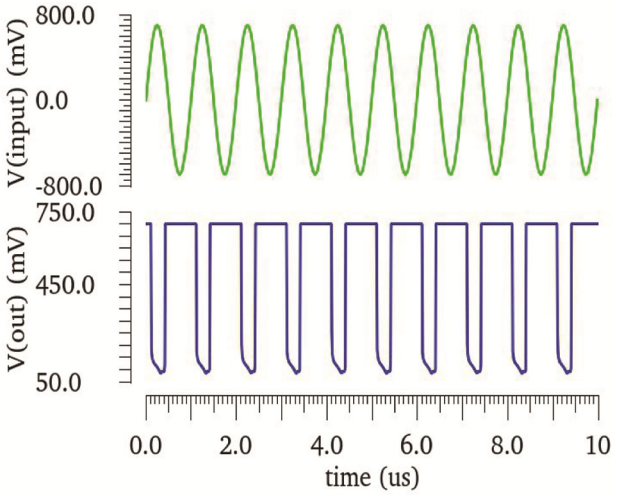

Fig. 6 — Waveform of SG LCNT FinFET Schmitt trigger.

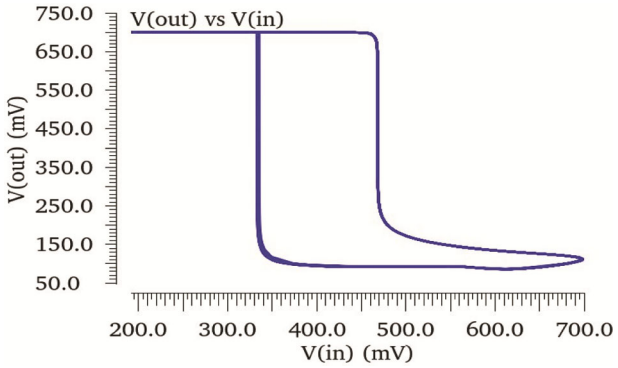

Fig. 7 — DC transfer characteristics of LCNT Schmitt trigger circuit at 7nm technology node.

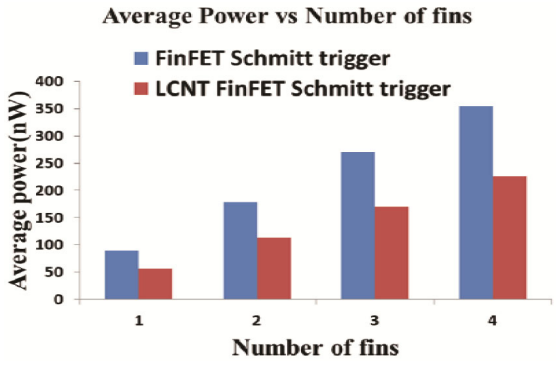

Fig. 8 — Effect of number of fins on Average Power.

of PVT variations, different PVT parameters are simulated as shown in Fig. 8, Fig. 9, Fig. 10 and Fig. 11.

The behavior of PVT variations is examined for FinFET Schmitt trigger and LCNT FinFET Schmitt trigger at 7nm technology node. Fig. 8 shows the effect of number of fins on Average power dissipation

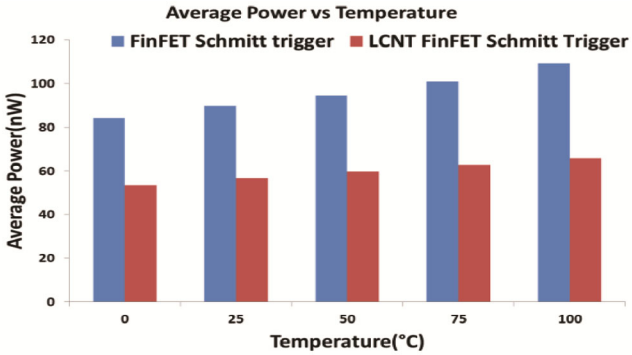

Fig. 9 — Effect of temperature on Average Power.

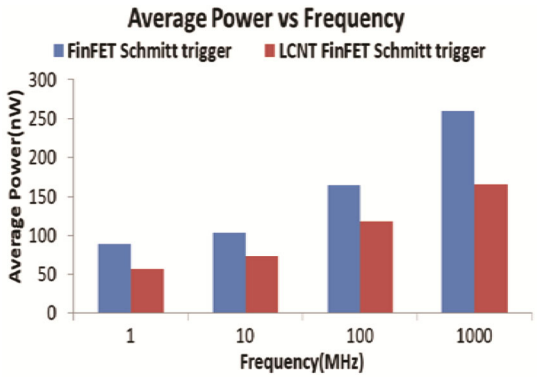

Fig. 10 — Effect of Frequency on Average Power.

in both FinFET Schmitt trigger and LCNT FinFET Schmitt trigger. It is obvious from the figure that increase in number of fins increases Average power dissipation. This is due to the reason that multi-fin structure of FinFET device increases the total drive current but at the same time it introduces coupling effect between nearby silicon fins. So there occurs a tradeoff between drive current capability and Average Power dissipation of FinFET device. Therefore, FinFET Schmitt trigger with fewer fins has less power dissipation as compared to one with higher number of fins. Therefore, devices with lesser number of fins show better performance but struggles with more intense hot carrier-induced degradation of device. This is due to the reduction of inversion charges in multi-fin, hence reduces impact ionization or low hot-carrier-induced degradation[20]. The environment effect on FinFET Schmitt trigger and LCNT FinFET Schmitt trigger is determined by temperature variation from 0 to 100 °C as shown in Fig. 9. With the increase in temperature, Average power dissipation increases due to the increase in carrier concentration by large amount at higher temperatures. Fig. 10 depicts the effect of frequency of operation of a device on Average power dissipation. With increase

Table 2 — Statistical Monte Carlo simulation data of Power Delay Product.

Performance Metric	FinFET Schmitt trigger without LCNT technique		FinFET Schmitt trigger with LCNT technique		%Change	
Power Delay Product	Mean (fJ)	Standard deviation (fJ)	Mean (fJ)	Standard deviation (fJ)	Δμ (%)	Δ σ (%)
	3.210	1.555	2.09	1.044	34.89	32.86

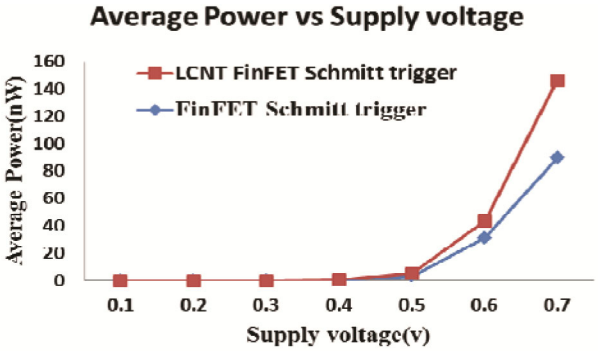

Fig. 11 — Effect of supply voltage on Average Power.

in frequency, power dissipation increases due to d irect dependency of dynamic power dissipation on frequency of operation. Fig. 11 shows the dependence of supply voltage on Average power dissipation. With the increase in supply voltage variation from 0.1 to 0.7 V, power dissipation shows a measurable increase due to direct relation between the two.

6 Monte Carlo Analysis of FinFET based Schmitt Trigger

PVT variations investigation is essential to look when the logic circuits are designed at lower technology nodes. For this statistical parameter like mean and standard deviation need to be analyzed. This can be done using Monte Carlo Approach[19]. The PVT variation largely effect the performance of FinFET Schmitt trigger at lower technology nodes and hence need to be analyze PVT variations in deep submicron region. The impact of these variations on power delay product is examined using Monte Carlo simulations. The simulations are performed for 5000 runs with 3σ Gaussian distribution. FinFET Schmitt trigger is considered as base and ± 10% variations of channel length of the device, channel width of the device, threshold voltages of device, external power supply voltage and temperature are considered. The LCNT Short gate FinFET Schmitt trigger provides better performance over short gate FinFET Schmitt trigger. The Monte Carlo analysis is performed by cadence virtuoso tool using ASAP7 PDK at 7 nm technology node. Table 2 shows the comparison of

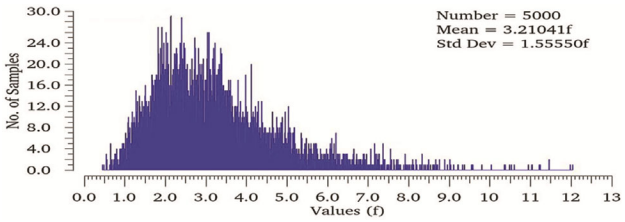

Fig. 12 — PDP of SG FinFET Schmitt Trigger.

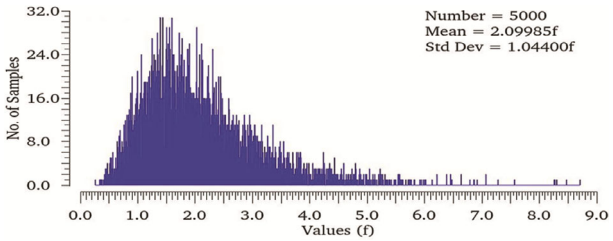

Fig. 13 — PDP of LCNT SG FinFET Schmitt Trigger.

LCNT FinFET Schmitt trigger and FinFET Schmitt trigger in terms of mean and standard deviation values of power delay product.

The histograms obtained from Monte Carlo analysis on power delay product are shown in Figs. 12 & 13 for FinFET Schmitt trigger and LCNT FinFET Schmitt trigger respectively. This whole examination makes us to conclude that FinFET based LCNT Schmitt trigger has better performance parameters like power dissipation and power delay product at 7nm technology node in comparison to the one without technique, moreover the proposed concept is less prone to PVT variation.

7 Conclusion

In this work, low power reliable Schmitt trigger circuit is investigated by FinFET device with and without LCNT technique. LCNT approach for FinFET logic circuits reduces leakage power dissipation to a large extent. FinFET Schmitt trigger is designed at 7nm technology node using LCNT leakage reduction technique. Various parameters like power delay product, average power dissipation and propagation delay is calculated. There occurs slight increase in propagation delay but the overall performance parameters are improved for LCNT FinFET Schmitt trigger. Average power dissipation

and power delay product is reduced by 36.97% and 35.6% respectively, hence makes the proposed design more energy efficient. Various parameters like number of fins, supply voltage, temperature and frequency are varied to check the effect of these parameters on Average power dissipation of FinFET Schmitt trigger and LCNT FinFET Schmitt trigger. PVT parameters are varied by ±10% at TT process corner for LCNT FinFET Schmitt trigger to check the reliability of FinFET Schmitt trigger for 5000 runs. Uncertainties for FinFET Schmitt trigger and LCNT based FinFET Schmitt trigger are calculated. The proposed design has lower value of uncertainty for PDP as compared to FinFET based Schmitt trigger without LCNT technique. Simulation results clearly depict that LCNT FinFET Schmitt trigger has lower power and PDP, hence improved performance in comparison to the conventional FinFET Schmitt trigger at 7 nm technology node.

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