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New Modified Voltage Differencing Voltage Transconductance Amplifier (MVDVTA) based Meminductor Emulator and its Applications

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This paper presents a new modified voltage differencing voltage transconductance amplifier (MVDVTA) based meminductor emulator circuit. The proposed emulator circuit is memristor-less, uses only a single active building block (ABB) and has simple circuitry. The MVDVTA based emulator design consists of only two capacitors and a single resistor. The performance of the proposed design has been verified over a wide frequency span. For simulation purpose LTSpice tool is used with 0.18µm CMOS technology. The proposed emulator has also been employed in chaotic oscillator and adaptive learning application circuit to verify its workability. The proposed design gives satisfactory performance for both the applications, hence confirming its functionality in practical environment.

Keywords: Modified voltage differencing voltage transconductance amplifier (MVDVTA); Meminductor; chaotic oscillator; adaptive learning

1 Introduction

Only three conventional circuit elements (resistor, capacitor, & inductor) were known till 1971. In 1971 Chua[1] gave the concept of another element named as memristor, which has memory characteristics along with resistive behavior. However, its first physical realization came much later in the year 2008, when HP Lab designed TiO_2 based physical model of memristor[2]. The notion proposed by Prof. Chua was extended further to introduce meminductor and memcapacitor in the year 2009[3]. These new elements come under a new category known as memelements. The memelements get their names from the basic elemental properties-resistance, inductance & capacitance along with the additional memory characteristic. The four circuit parameters which defines these memelements are q (electric charge), σ, Φ (induced flux), and ρ, where, σ,Φ and ρ are calculated as the time integral of charge, voltage, and flux respectively. The relation among these circuit parameters for three memelements is shown in Fig. 1. These elements, specifically meminductor and memcapacitor have gained a lot of focus due to their wide range of applications, dominantly in the field of neural network. The physical realization of these elements has not been available yet, so various emulator circuits have been proposed to mimic their behaviour. The recent literature suggest that these emulators are realized using various active building blocks (ABBs) and can be broadly classified into two categories – one which consists of memristor and a mutator circuit and other category which is memristor-less. The first emulator proposed in 2010[4] consists of op-amp, memristor with potentiometer and an analog-to-digital converter. After this a mutator circuit consisting of current conveyor (CC) and operational transconductance amplifier has been reported[5], which transforms memristor to meminductor and memcapacitor.

In the year 2013, SPICE model for these elements was reported[6]. Another mutator based emulator circuit mimicking the behavior of meminductor and memcapacitor has been reported[7]. The circuit consists of second generation current conveyor (CCII), memristor and multiplier along with capacitors and resistors. After this a memristor-less emulator[8] consisting of four AD844s, two op-amp, multipliers, resistors and capacitors was reported in the year 2014. Two charge controlled memristor-less meminductor emulators have been proposed in[9-10]. Their design constituted of op-amp, multiplier, AD844 along with resistors and capacitors. In year 2016, a flux controlled emulator was reported[11]. The emulator was memristor-less using four op-amps, two multipliers along with multiple passive elements capacitors and resistors. Another meminductor and

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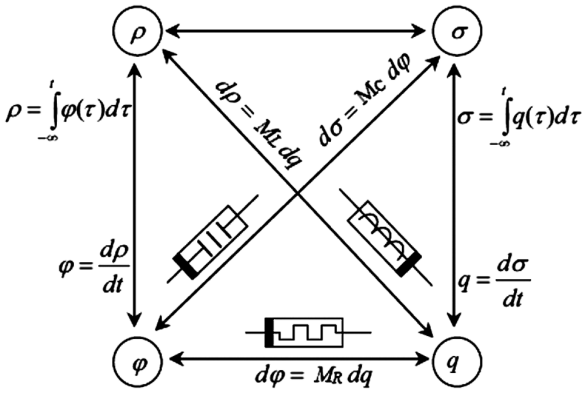

Fig. 1 — Relation between circuit parameters for memelements.

memcapacitor emulator was reported in[12]. Its design consists of inductor and resistor with a single OTA and a voltage reference. Further research gave a universal emulator[13] capable of realizing both grounded and floating meminductor and memcapacitor. The universal emulator design was based on current conveyors, AD633 analog multiplier and multiple resistors and capacitors. Furthermore, a meminductor emulator was reported in[14] for high frequency applications. The design of this emulator uses two voltage differencing transconductance amplifier (VDTAs) and two capacitors. A current buffered transconductance amplifier based mutator circuit was reported in recent literature[15]. This mutator design also involves memristor and capacitors. After this an operational transconductance amplifier (OTA) based electronic tunable emulator using multiplier circuit with resistors and capacitors was reported[16]. A voltage differencing current conveyor (VDCC) based mutator circuit was reported in[17]. The mutator in this circuit transforms the memristor to meminductor and memcapacitor.

From recent literature exploration, it has been concluded that majority of meminductor emulators are based on mutator circuit transforming memristor to meminductor. A few memristor-less emulators that have been reported in literature have complex circuitry, as their designing involves analog multipliers and excessive count of active and passive components. Furthermore, some of the emulators reported in recent literature uses multiple combinations of active building blocks leading to complex architecture. This paper aims at proposing a new meminductor emulator which is memristor-less and does not require any complex multiplier circuit. Moreover, the proposed emulator uses a single active building block along with two capacitors and single resistor leading to a simple circuitry.

In this paper, section 2 covers a brief review of meminductive system and characteristic of modified voltage differencing voltage transconductance amplifier (MVDVTA). In section 3, description of proposed meminductor emulator has been provided. The simulation results for the proposed emulator have been presented in section 4. The section 5 covers a brief comparison of the proposed emulator with already reported emulators. Section 6 describes the application circuit and their simulation results of the proposed meminductor emulator and finally section 7 concludes the work.

2 Review of Meminductive System and MVDVTA Characteristics

2.1 Review of Meminductive System

Meminductor possesses inductive behaviour with additional memory characteristics. The meminductive behaviour can be explained with the help of variables ρ and q. Eq. (1) and (2) define ρ as time integral of flux and q as time integral of current[18,19]:

$$\rho = \int_{\infty}^{t} \Phi(t).\,dt \quad \ldots(1)$$

$$q(t) = \int_{\infty}^{t} I(t).\,dt \quad \ldots(2)$$

The meminductance (M_L) of a meminductor is given as[18,19]:

$$\Phi(t) = M_L\, I(t) \quad \ldots(3)$$

where, I(t) is current and Φ(t) is induced flux represented mathematically as[18,19]:

$$\Phi(t) = \int_{\infty}^{t} V(t).\,dt \quad \ldots(4)$$

2.2 MVDVTA Characteristics

The modified voltage differencing voltage transconductance amplifier (MVDVTA) is an active building block proposed by H Alpasalan in 2016[20]. Its block diagram is shown in Fig. 2(a). Its terminals are: P,N,X,Y0,O_C,V,V_C, Z+ and Z-. The voltage at X terminal is the difference between Y0 and V terminals. The terminal O_C acts as an auxiliary terminal providing positive/negative current. At output stage, the current at X terminal is transferred to Z terminals. The terminal V_C provides bias voltage for the MVDVTA block. To widen the application area of MVDVTA, it can be modified to get multiple output terminals by adding current repeaters.The CMOS based implementation of MVDVTA is shown in Fig. 2(b). The port equations of MVDVTA are given as[20]:

$$I_P = I_N = 0 \quad \ldots(5)$$

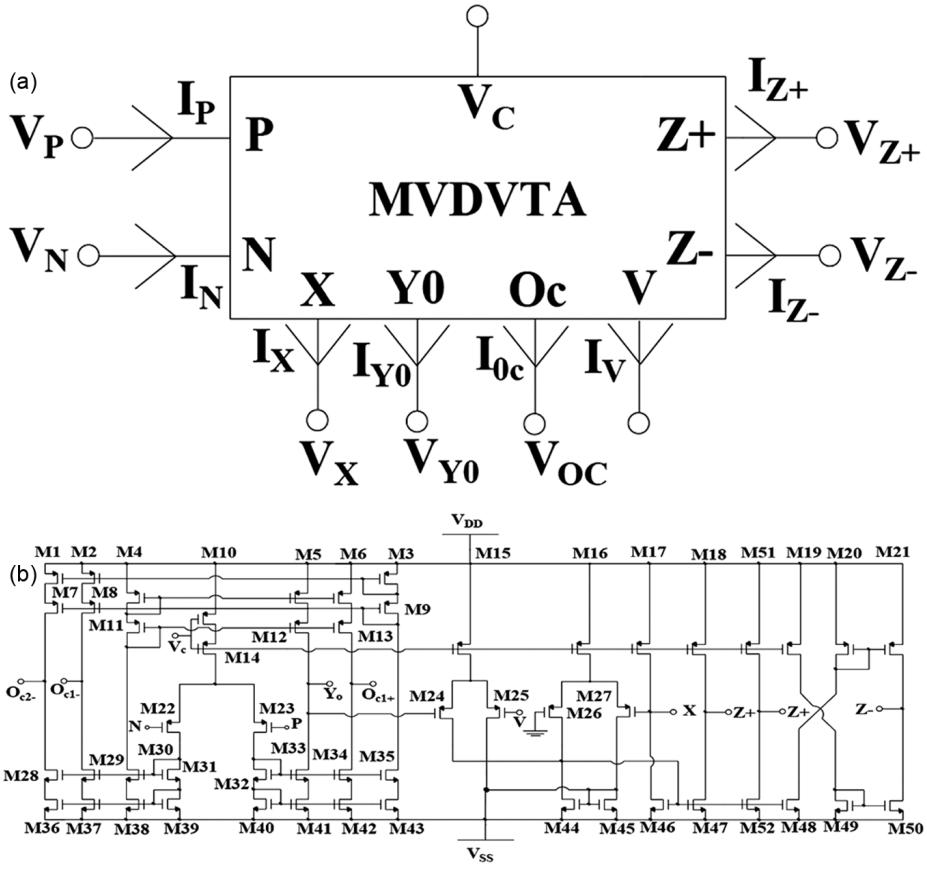

Fig. 2 — (a) MVDVTA block[20], (b) CMOS based implementation of multiple outputs MVDVTA[20].

$$I_{Y0} = g_m(V_P - V_N) \quad \ldots(6)$$

$$I_{OC\pm} = \pm g_m(V_P - V_N) \quad \ldots(7)$$

where, g_m is transconductance given by:

$$g_m = \frac{k}{\sqrt{2}}(V_C - V_{ss} - 2V_{th}) \quad \ldots(8)$$

$$V_X = V_{Y0} - V \quad \ldots(9)$$

$$I_{z\pm} = \pm I_X \quad \ldots(10)$$

3 Proposed Meminductor emulator

This section briefly describes the circuit of proposed meminductor emulator. The design consists of a single MVDVTA block with two grounded capacitors and one grounded resistor. The proposed emulator is shown in Fig. 3. Here input voltage is provided at P and N terminals, which generates a proportional current at Y0 and O_C terminals. The capacitor C_1 is connected to Y0 terminal and V terminal is grounded. The difference of voltage between Y0 and V is transferred to X terminal. This voltage causes a current I_X through resistor R connected at X terminal, which gets transferred to Z± terminals with opposite polarity. The capacitor C_2 is connected at Z+ terminal, generating voltage which controls the DC voltage V_C for MVDVTA block. The feedback is provided to input terminals P & N from Z+ and Z- respectively, due to which input current I_{in} is proportional to the input flux. Mathematical analysis of the proposed emulator is given below:

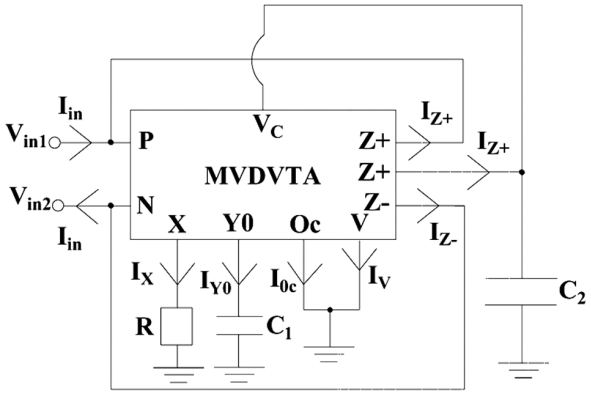

Fig. 3 — Proposed meminductor emulator.

Analysis of Fig. 3 and using Eq. (6), current and voltage at Y0 terminal are given as:

$$I_{Y0} = g_m(V_{in1} - V_{in2}) \quad \ldots(11)$$

$$V_{Y0} = \frac{1}{C_1}\int I_{Y0}\,.dt \quad \ldots(12)$$

From Fig. 3, it can be observed that terminal V is grounded, therefore using Eq. (9), voltage at X terminal can be given as:

$$V_X = V_{Y0} = \frac{1}{C_1}\int I_{Y0}.dt \quad \ldots(13)$$

Taking the value of I_{Y0} from Eq. (11) and putting it in Eq. (13) gives:

$$V_X = \frac{g_m}{C_1}\int (V_{in1} - V_{in2}).dt \quad \ldots(14)$$

Further using Eq. (10), current through terminals Z± can be given as:

$$I_{Z\pm} = \pm\frac{g_m}{C_1 R}\int (V_{in1} - V_{in2}).dt \quad \ldots(15)$$

The time integral of input voltage can be written as input flux, as given in Eq. (4), so Eq. (15) can be modified as:

$$I_{Z\pm} = \pm\frac{g_m}{C_1 R}\varphi_{in}(t) \quad \ldots.(16)$$

From Fig. 4, the bias control voltage V_C can be given as:

$$V_C = \frac{1}{C_2}\int I_{Z+}\,.dt \quad \ldots(17)$$

Using the value I_{Z+} from Eq. (16) in Eq. (17) yields:

$$V_C = \frac{g_m}{C_2 C_1 R}\int \varphi_{in}\,(t).dt \quad \ldots(18)$$

Using Eq. (1), Eq. (18) can be re-written as:

$$V_C = \frac{g_m}{C_2 C_1 R}\rho_{in}(t) \quad \ldots(19)$$

For the proposed emulator, it can be observed from the Fig. 3 that input current I_{in} =-I_{Z+}, hence

$$I_{in} = -\frac{g_m}{C_1 R}\varphi_{in}(t) \quad \ldots(20)$$

Using Eq. (8), Eq. (20) can be written as:

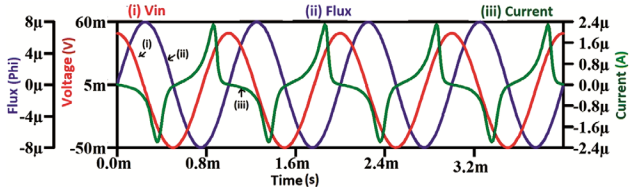

Fig. 4 — Transient response.

$$I_{in} = -\frac{1}{C_1 R}\frac{k}{\sqrt{2}}(V_C)\varphi_{in}(t)$$

$$-\frac{1}{C_1 R}\frac{k}{\sqrt{2}}(-V_{SS} - 2V_{th})\varphi_{in}(t) \quad \ldots(21)$$

The value of V_C can be substituted from Eq. (19), then Eq. (21) yields:

$$I_{in} = -\frac{1}{C_1 R}\frac{k}{\sqrt{2}}(-V_{ss} - 2V_{th})\varphi_{in}(t)$$

$$-\frac{1}{C_1 R}\frac{k}{\sqrt{2}}\left(\frac{g_m}{C_2 C_1 R}\rho_{in}(t)\right)\varphi_{in}(t) \quad \ldots(22)$$

On comparing Eq. (22) with relation between input flux and current as represented by Eq. (3), inverse meminductance (M_L^{-1}) can be represented as:

$$M_L^{-1} = \frac{1}{C_1 R}\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th})\varphi_{in}(t)$$

$$+\frac{1}{C_1 R}\frac{k}{\sqrt{2}}\left(-\frac{g_m}{C_2 C_1 R}\rho_{in}(t)\right)\varphi_{in}(t) \quad \ldots(23)$$

From Eq. (23) it can be observed that the meminductance of proposed design consists of two terms – one is variable term dependent on the input flux $\left(-\frac{1}{C_1 R}\frac{k}{\sqrt{2}}\left(\frac{g_m}{C_1 C_2 R}\rho_{in}(t)\right)\right)$ and second term$\left(\frac{1}{C_1 R}\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th})\right)$is the fixed term dependent on circuit and device parameters.

4 Simulation Results and Discussion

For simulation purpose LT Spice tool with TSMC 180nm model file for CMOS technology has been used. Table 1 shows the aspect ratios for CMOS based implementation of MVDVTA provided in Fig. 2(b). The bias voltages are taken as ±0.9V. To perform various analyses capacitors C_1 and C_2 are fixed at 300pF and 400pF respectively, along with resistor R fixed at 5kΩ.

For transient response, the proposed emulator has been simulated with a sinusoidal bipolar input with amplitude 50mV and frequency 1 kHz. The transient response is plotted between (i) Vin (ii) Flux (iii) Current as shown in Fig. 4. Thorough observation of the response reveals that phase of input current and input flux lags behind the phase of input voltage.

Table 1 — Aspect ratios for CMOS based implementation of multiple outputs MVDVTA.

Transistor type	Transistor Number	W(µm)	L(µm)
PMOS	M1-M27, M51	13	1.04
NMOS	M28-M50, M52	3.9	1.04

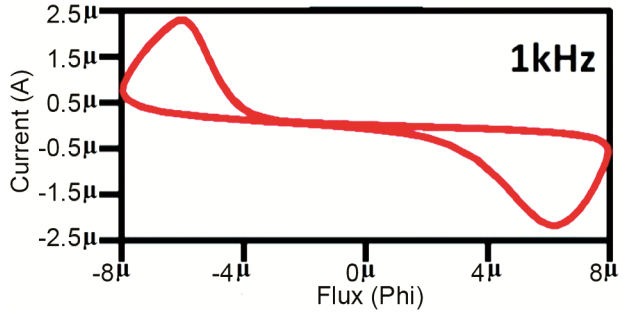

Fig. 5 — PHL plot in current *vs* flux plane.

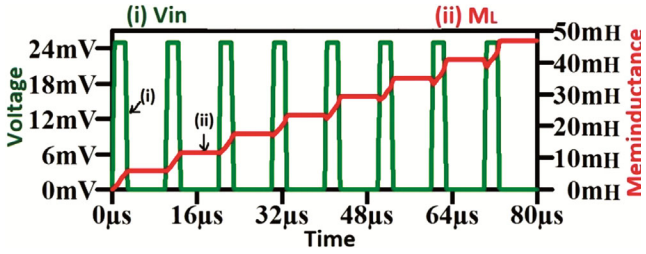

Fig. 6 — Non-volatility response.

Table 2 — Value of passive components at different frequencies.

Frequency	C_1(pF)	C_2(pF)	R(kΩ)
1kHz	300	400	5
2kHz	150	400	5
5kHz	68	400	5
10kHz	32	400	5
25kHz	10	100	1
50kHz	6	100	1
100kHz	3	100	1
200kHz	1.5	100	1
300kHz	0.9	100	1
500kHz	0.5	100	1

The meminductive behavior of the proposed design of meminductor emulator is examined by simulating the circuit with a bipolar sinusoidal input of amplitude 50mV and frequency 1 kHz. The pinched hysteresis loop (PHL) obtained in flux *vs* current plane is shown in Fig. 5. The obtained PHL confirms the meminductive behavior of the proposed emulator.One of the most critical characteristics of a mem-element is its non-volatility behaviour. The non-volatility characteristic is confirmed by simulating the proposed design with a pulse input of amplitude 25mV. The 'ON' period of the input pulse signal is set as 2µs and its time period is 10µs.The variation of meminductance is shown in Fig. 6. From the observed response, it can be easily deduced that during the ON period the value of meminductance (M_L) gradually increases and the value is retained for the remaining OFF period of each pulse.

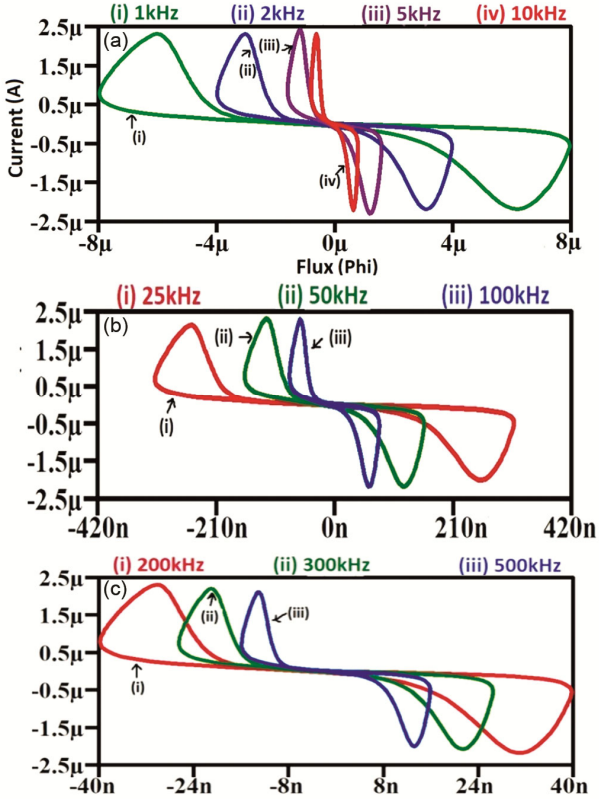

Fig. 7 — (a) PHL curves observed for sinusoidal input signal of frequency: (a) (i) 1kHz, (ii) 2kHz, (iii) 5kHz (iv) 10kHz; (b) (i) 25kHz, (ii) 50kHz, (iii) 100kHz (c (i) 200kHz, (ii) 300kHz, (iv) 500kHz.

The behavior of proposed design is analysed over a range of frequency. For this analysis the capacitor C_1 and C_2 are suitably scaled along with resistor R. The corresponding value of three components at various frequencies is summarized in Table 2. The obtained PHL response over the frequency range of 1 kHz to 500 kHz is shown in Fig. 7.

5 Comparison of Proposed Emulator with Available Emulators

To prove the usefulness of the proposed design, it is compared with the emulators already available in literature. The comparison is shown in Table 3.The key parameters used as basis of comparison are – maximum operating frequency, count of active and passive elements used.

6 Applications of Proposed Meminductor Emulator

For confirming the workability of proposed emulator, two application circuits namely - chaotic oscillator and adaptive learning circuit along with their simulation results are presented in this section.

Table 3 — Comparison table between proposed emulator and already existing emulator.

Reference	Active elements	Passive elements	Maximum Frequency
[4]	1 op-amp	1MR, 1R, 1C	4Hz
[7]	3 CFOAs	1MR, 2R, 1C	20Hz
[8]	2 op-amps, 4 CFOAs, 1 multiplier	5R, 1C	36Hz
[9]	1 multiplier, 3 op-amps,	2 R, 1 C, 12 MOSFETs	300Hz
[10]	1 Adder,1 multiplier, 4 CCIIs	3 R, 1 C	5Hz
[11]	2 multipliers, 4 op-amp	8 R, 2 C	180Hz
[12]	1 voltage reference,1 OTA	1 L, 1 R, 1 C	500Hz
[13]	1 op-amp, 1 AD633, 5 AD844s	5 R, 1 C	5kHz
[14]	1 multiplier, 2 VDTA	2 C	1MHz
[15]	1 CBTA	1 MR, 1C	100kHz
[16]	2 multipliers, 2 OTAs	2 R, 2 C	10kHz
[17]	1 VDCC	1MR, 1C	700kHz
Proposed	1MVDVTA	2C, 1R	500kHz

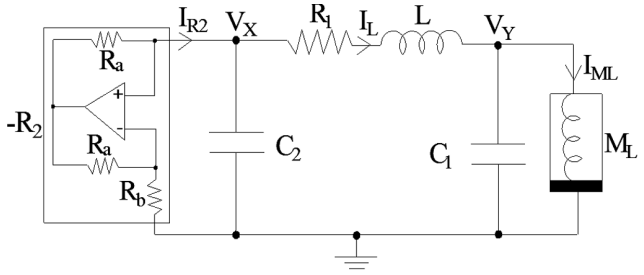

Fig. 8 — Chaotic oscillator circuit.

6.1 Chaotic Oscillator

In this sub-section, chaotic oscillator has been realized using the proposed meminductor emulator. For the generation of chaotic waveforms, Chua's oscillator is considered to be one of the simplest circuit[21,22]. A simple form of Chua's oscillator is presented in Fig. 8. The oscillator consists of a negative resistance ($-R_2$) realized using op-amp based negative impedance converter, one inductor (L), two capacitors (C_1 & C_2), one meminductor (M_L) and a resistor (R_1). For this simple oscillator the four state variables are - node voltages across two capacitors (V_X & V_Y), and current through inductor (I_L) and meminductor (I_{ML}).

The state space dynamics of this meminductor-based oscillator can be represented by first order differential equation given as follows:

$$C_2 \frac{dV_X}{dt} = -I_L + \frac{V_X}{R_2} \quad \ldots(24)$$

$$C_1 \frac{dV_y}{dt} = I_L - I_{ML} \quad \ldots(25)$$

$$L \frac{dI_L}{dt} = V_X - V_Y - I_L \cdot R_1 \quad \ldots(26)$$

$$M_L \frac{dI_{ML}}{dt} = V_Y \quad \ldots(27)$$

The op-amp based negative impedance converter realizes the negative resistance ($-R_2$) with $R_a = R_b = 2k\Omega$. The value of remaining passive components is set as L=120mH, C_1=65nF, C_2=10nF and R_1=100Ω. The 2-D projection plots obtained for various state variables are exhibited in Fig. 9.

6.2 Adaptive Learning Circuit

In this sub-section, the proposed emulator is used to realize an adaptive learning circuit. The adaptive learning circuit is used to mimic the locomotive response of amoeba towards its environmental change[23-25]. The circuit is realized using a resistor (R), capacitor (C) and meminductor (M_L) as shown in Fig. 10. Learning and remembrance are two important factors included in the behavioural response of amoeba towards its environmental changes. Amoeba learns and remembers from its environmental change, so that in future for similar environmental change it can produce similar response. The variation of meminductance with applied voltage can be attributed with tuning of the adaptive learning circuit. The circuit given in Fig. 10 uses Vin to emulate temperature gradation and the corresponding behavioral response is represented by Vout.

The component values are set as R=0.5kΩ and C =10nF. From the response curves shown in Fig. 11, it is clearly observed that Vout varies till (0.5μs) in accordance with variation in Vin. It is analyzed that for variation around (2.5 μs) the adaptive learning circuit remembers its previous response. The learning and remembrance process of amoeba is equivalent with this response.

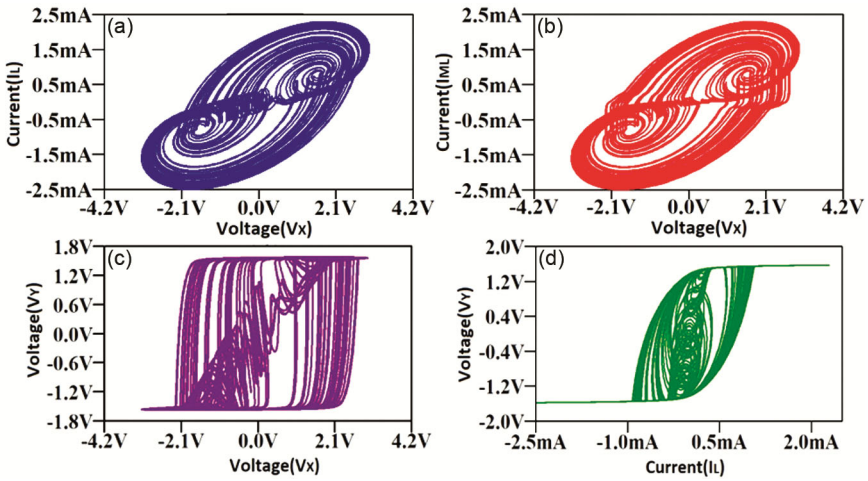

Fig. 9 — 2-D Plots for Chaotic oscillator circuit between (a) V_X and I_L (b) V_X and I_{ML}(c) V_X and V_Y (d) I_L and V_Y.

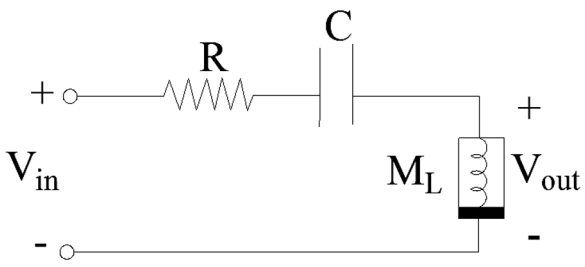

Fig. 10 — Adaptive learning circuit.

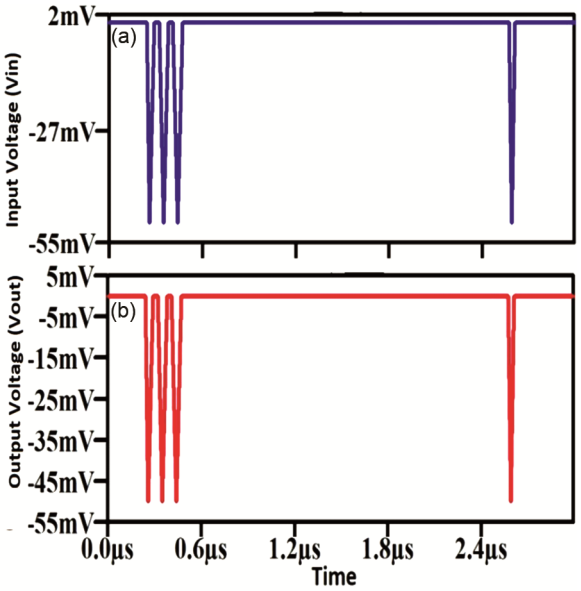

Fig. 11 — Adaptive learning response (a) Input (b) output.

7 Conclusions

In this paper, a new MVDVTA based meminductor emulator has been proposed. The proposed emulator is unique as it is memristor-less and has simpler circuitry. The proposed design uses a single active building block, two grounded capacitors and one grounded resistor. The emulator neither requires any complex circuitry like analog multiplier, divider *etc*., nor combination of active building blocks. The emulator provides PHL response for a wide frequency span ranging from 1 kHz to 500 kHz. The emulator also satisfies the non-volatility characteristic of meminductor. The proposed design gives satisfactory results for practical application circuits- chaotic oscillator and adaptive learning which confirms the workability of the design in practical environment.

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